Memristive circuit development for neuromorphic computation applications

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Theses of the PhD dissertation

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1 Introduction

Since the theoretical [1] and practical [2] discovery of memristors, they have been extensively studied [3, 4, 5] as elementary building blocks for artificial intelligence and neuromorphic computing applications. These devices can change their resistive state in response to applied voltage or current and retain their state without external power. Key properties like non-volatility and synapse-like behavior have made them promising for neuromorphic computing and memory storage applications. Although not all resistive switching devices align exactly with Chua's original model, they are generally referred to as memristors [6].

Unlike traditional binary memory, memristors can store information across multiple resistive states, which makes them suitable for analog data processing and brain-inspired computing. Consequently, researchers are exploring their benefits, such as low power consumption, non-volatility, and high-density storage. In digital systems, memristors offer a compact alternative to traditional CMOS technology, with the potential to store multiple bits per device by leveraging multistate behavior. This could lead to significant energy savings, making memristors ideal for energy-efficient computing.

In neuromorphic computing, memristors can emulate biological synapses more effectively than traditional components. Analog Purpose Memristors (APMs) mimic synaptic plasticity by continuously changing resistance, which is essential for adaptable neural networks. Additionally, their non-volatility ensures that information is retained without constant refreshing, unlike traditional dynamic RAM, making them useful for both memory and computation.

Despite their potential, implementing memristors in practical computing systems comes with challenges. One major issue is accurately measuring their resistive states and developing reliable models to predict their behavior. Memristors often exhibit non-linear and unpredictable voltage-current characteristics, complicating consistent state characterization [7]. Different memristors operate on varying principles, making it difficult to create universal models applicable across devices. Thus, more empirical data is needed to refine models for simulations and real-world use.

Another challenge involves the variability and unreliability of memristive devices. Due to imperfections in materials, environmental factors, and the stochastic nature of resistive switching, memristors can exhibit significant performance differences, even between identical devices [8]. This variability can hinder consistency in applications, especially when precise resistance levels are necessary. Additionally, resistive drift—where a memristor's

resistance changes over time without external stimuli—introduces further unpredictability [9].

In neuromorphic computing, variability and drift complicate the use of memristors as reliable synaptic elements. Neuromorphic systems often require memristors to switch between a wide range of resistive states in a controlled and consistent manner [10]. Variability and drift can undermine their analog behavior, potentially degrading the performance of the entire system. Ensuring that memristors reliably emulate synaptic plasticity remains a significant challenge.

My work focused on developing better measurement techniques, designing more effective circuits, and testing real-world applications to overcome the limitations and unpredictability of memristors. To address these challenges, I adopted a comprehensive approach aimed at improving the reliability, measurement, and application of memristors in neuromorphic computing.

To tackle measurement and modeling challenges, I designed and built a custom measurement environment tailored for memristive devices. This setup allowed me to capture detailed empirical data on resistive switching behavior, enabling more accurate models. By analyzing voltage-current relationships and transient behaviors, I developed improved models that better reflect the non-linear and stochastic characteristics of real-world memristors. These models can serve as the basis for future simulations and predictions, helping to understand memristor behavior across various conditions [2, 11].

In response to device variance and unreliability, I built and tested multiple memristor network circuits aimed at reducing variability and improving consistency [12]. I developed a circuit that transforms unreliable Binary Purpose Memristors (BPMs) into more reliable Digital Purpose Memristors (DPMs), which can exhibit multistate behavior [13]. I later designed an improved version that further enhanced reliability by arranging the memristors in a grid, mitigating the effects of variability and resistive drift. This configuration produced a more stable output, demonstrating that combining unreliable devices can create a more reliable system.

In exploring practical applications, I built a memristor-based Cellular Neural Network (CNN) designed to leverage the analog nature of memristors for low-power computations. I developed a template for the CNN that implements the XOR logical operation, a key function in many computational tasks. This proof of concept shows the potential of memristor-based systems for neuromorphic computation, offering a foundation for further research in the field.

In conclusion, memristors hold significant promise for diverse applications, from high-density memory storage to neuromorphic computing. However, to fully harness their potential, challenges related to measurement, device variance, and practical implementation must be addressed. Through this research, I have made progress in tackling these challenges by developing improved measurement techniques, designing circuits that reduce variability, and building practical applications such as a Memristor Cellular Neural Network. This work advances the understanding and reliability of memristor-based systems, paving the way for more energy-efficient and robust technologies in both memory and computation.

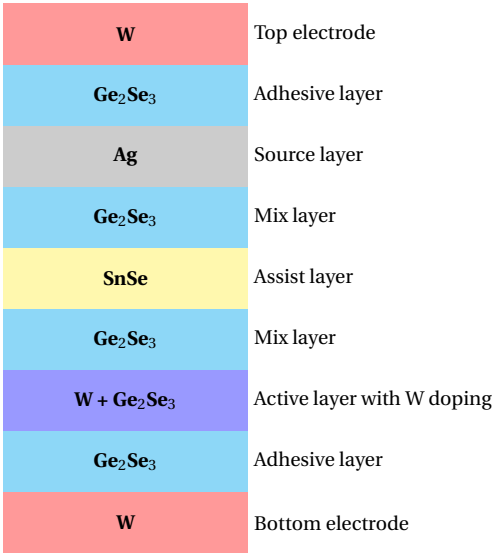


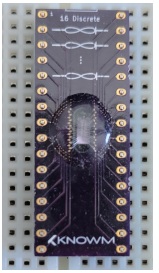
Figure 1: The structure of the Knowm SDC memristor with Tungsten dopant. This type of device was used in the memristor characterisation experiments.

2 Methods

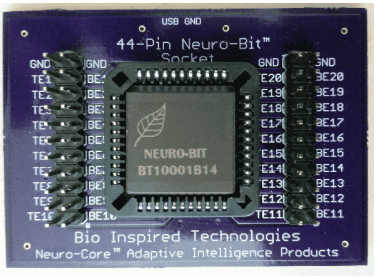
In my research, I examined the resistive switching behavior and reliability of Knowm's Self-Directed Channel (SDC) memristors. The structure of these memristors is illustrated in Figure 1. These devices consist of several layers, with the "active" layer as a key switching occurring in the doped Ge_2Se_3 layer. This layer is responsible for the device's resistive state changes, which

happen through the movement of silver ions within the structure. The shifting of ions in and out of conductive channels is what allows the memristor to alter its resistance, forming the basis of its operation.

I used two different subtypes of the SDC memristor in my work: Tungsten-doped and Carbon-doped. These only differ in the dopant material, which always occurs in the active layer shown in Figure 2. For single-device characterization and modeling, I worked with the Tungsten-doped SDC memristor, shown in Figure 2a, which exhibited more consistent performance and allowed for a clearer study of memristive switching behavior. For the memristor network experiments, I employed the Carbon-doped SDC memristor, shown in Figure 2b. This version showed greater variability in its resistive states, making it better suited for testing methods aimed at addressing and reducing variability.



(a) Contains 16 independent SDC W memristors.



(b) Contains 20 independent SDC C memristors.

Figure 2: Images of the analyzed memristor chips.

The measurement setup differed for the two types of experiments. For single-device measurements and modeling, I used a **Keysight InfiniiVision MSO-X 3054A** oscilloscope. This was connected to a laptop running **NI LabVIEW**, which allowed for automated control of the experiment, regulation of input voltages, and real-time data collection from the memristor. Maintaining a controlled environment was essential for ensuring accurate measurements and reducing external noise that could affect the memristor's performance.

For the memristor network experiments, which were focused on the Carbon-doped SDC memristors, I used an **NI ELVIS II+** measurement instrument. Like the single-device experiments, the NI ELVIS II+ was controlled via **NI LabVIEW**, ensuring consistent and reproducible input signals and automated data acquisition.

I also used a TaO_x memristor model for memristor cellular neural network (MCNN) simulations. This was done in order to get results directly comparable to existing MCNN simulation results.

The data collected from both single-device and network measurements was processed using **MatLab** and **Python3**. Custom scripts were written to handle the data collected from the oscilloscope and the NI ELVIS II+, allowing for efficient manipulation and analysis of the datasets generated during the experiments and simulations.

3 Summary of new scientific results

Thesis group I.

1. I developed a specific measurement environment to accurately map the characteristics of the Knowm SDC W memristor, enabling a detailed modeling of the memristor's state and resistance-voltage behavior.

1.1. I designed and implemented a custom measurement framework for modeling the behavior of the Knowm SDC W memristor. The framework contains a minimal number of noise-inducing components, making it particularly suitable for precise characterization.

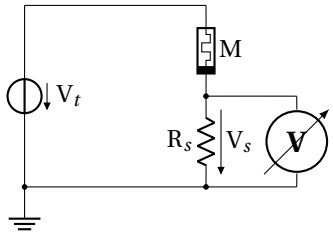


Figure 3: Single memristor state analysis measurement circuit.

The measurement setup consists of a single "Knowm SDC W" memristor, in series with a $100k\Omega$ resistor, R_s, as shown in Figure 3. The main advantage of this measurement setup is its simplicity. There are minimal parasitic capacitances and other noise inducing elements. The disadvantage is that it does not allow for a constant voltage applied across the device. As the state of the memristor changes, the voltage-current relationship also changes, making it challenging to maintain a constant voltage across the device during

measurements. However, in this scenario low voltages are being used across the device, therefore memristor state change is minimal.

1.2 Based on measurements, I characterized the voltage dependence and non-linearity of the resistance of the Knowm SDC W memristor. I created an accurate resistance model using non-linear parameter fitting

To gather information about the state the memristor is set to some arbitrary state between measurements and a low amplitude $1\,kHz$ triangle signal is applied as input (V_t) in order to to read the state without disrupting it. The voltage data are acquired at high resolution setting, which is using a temporal averaging to reach higher precision. With this approach, a diverse data can be collected about the voltage-current characteristics of the device.

After collecting the data from the oscilloscope I used an automated fitting procedure to attempt to eliminate systematic measurement offsets for the voltage and the current values.

The small-signal memristor model can be calculated using the following equations:

$$i_{mem} = \frac{V_s}{R_s} \tag{1}$$

$$v_{mem} = V_t - V_s \tag{2}$$

$$r_{mem} = \frac{v_{mem}}{i_{mem}} = R_s \cdot \frac{V_t - V_s}{V_s} = R_s \cdot \left(\frac{V_t}{V_s} - 1\right), \tag{3}$$

where v_{mem}, i_{mem} and r_{mem} are the memristor voltage, current and resistance respectively.

Initial experiments conducted on the Ge_2Se_3 devices confirmed the characteristic to be exponential in nature. The VI characteristic was also non-symmetric for positive and negative biases.

I chose to model the switching as an Ohmic component in parallel with both a forward and reverse diode, which accounted for both the exponential nature of the model, and the asymmetric characteristic. The Ohmic component can also be considered a first-degree (linear) approximation of sinh tunneling switching behaviour.

Eq. 4 describes the two parallel Schokley diodes with opposing orientations:

$$I_d = \alpha_1 \cdot (e^{\beta_1 \cdot v(t)} - 1) + \alpha_2 \cdot (1 - e^{-\beta_2 \cdot v(t)}), \tag{4}$$

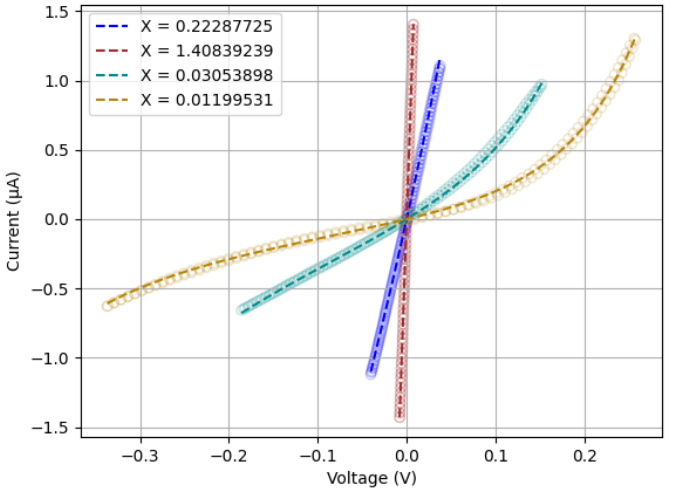


Figure 4: The faint colored bands represent the measurements with different initial memristor state, and the thin dashed line shows the result of the modeling.

The term containing α_1 and β_1 defines the characteristics of the memristor's resistance decrease, while the term containing α_2 and β_2 defines the characteristics of the memristor's resistance increase.

Eq. 5 is the final form of the model

$$i(x, v(t)) = x \cdot (G_p \cdot v(t) + I_d) \,, \tag{5}$$

where G_p is state independent variables and $x \in (0, 10]$ is a parameter that depends on the memristor state.

Table 1: Result of the model parameter fitting.

Model parameters				
α_1	α_2	β_1	β_2	G_p
0.8	1.6	12	4.5	7

In choosing model parameters (α_1, α_2, β_1, β_2 and G_p), we seek to min-

imise the fitting error of the model. Using an iterative grid search method, I tested several sets of model parameters, while the state variable x was estimated for each measurement using the Levenberg–Marquardt damped least squares method. The model parameter values can be seen on Table 1. This model has a mean average error less than 18 nA compared to the measurement data.

The result can be seen on Figure 4. It showcases the model with a few example measurements from the state characterisation dataset.

Publications supporting Thesis group I.: [J2,C1,C2,C7,C8,C9].

Thesis group II.

2. I designed and implemented networks of different topology consisting of several memristors and compared them to a single memristor device to demonstrate that the networks exhibit lower cycle-to-cycle variance than the individual device.

2.1 I designed and implemented a framework for measuring memristor networks to demonstrate that it is possible to emulate a single memristor by connecting multiple memristors in a grid, and that the parameters of the emulated memristor are more robust.

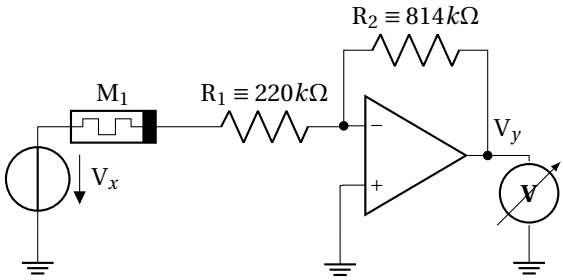


Figure 5: Measurement environment circuit. The measurement setup consists an amplifier circuit as a current controlled voltage source and a current regulator resistor. The used amplifier is a "TL082". The applied voltage V_x was strictly between −2.5V and 2.5V. The memristor symbol represents either a single memristor or a network of memristors depending on the measurement.

In the previous point, control was not emphasized as much because the

focus was primarily on exploration. The goal was to gather as much data as possible to gain a broad understanding of the system.

In this point, however, precision was prioritized to improve the reliability of the results. The designed measurement setup can be seen on Figure 5. The use of an operational amplifier enhanced measurement accuracy by amplifying the signal and reducing environmental noise. However, this approach introduced offset errors due to the presence of parasitic capacitance's inherent in the circuit components. These capacitance's affected the readings, requiring careful calibration and consideration in the interpretation of the results.

The cycle-to-cycle variance describes the variability (dispersion) between the conductive states that arise as a result of repeated voltage or current pulses applied to program the memristor. This variance measures the cycle-to-cycle deviation of the written ("SET") and erased ("RESET") states, characterizing the stability and predictability of the device or network.

The experimental setup (Figure 6.) utilized an "NI ELVIS II+" signal generator and measurement device, which was operated through LabVIEW software. This platform allowed for precise control of the experimental conditions and automated data collection, enhancing the consistency and repeatability of the measurements.

2.2 I conducted measurements on memristor networks made of 16 "Knowm SDC C" memristors and compared them with measurements from individual devices. I found that the cycle-to-cycle variance of the emulated device is smaller than that of the individual device.

Measurements were conducted on two memristor network circuit topologies (checkerboard-like and H-fractal), with previously introduced [12] corresponding simulation results. The H-fractal (Figure 7e & Figure 7f) and checkerboard-like (Figure 7c & Figure 7d) topologies both produced comparable results, supporting the validity of testing both configurations experimentally. In simulations with high defect probability, the checkerboard-like topology showed slightly better performance. The sampling frequency for all measurements was $500k\mathrm{S}/s$, and the state of each device was reset to OFF before each measurement. The result can be seen on Figure 2. The numerical results on Table 2.

2.3 Based on the measurement results, I designed, implemented, and tested a new network topology that further reduced the cycle-to-cycle variance of the device emulated by the network. I also introduced a 3-dimensional net-

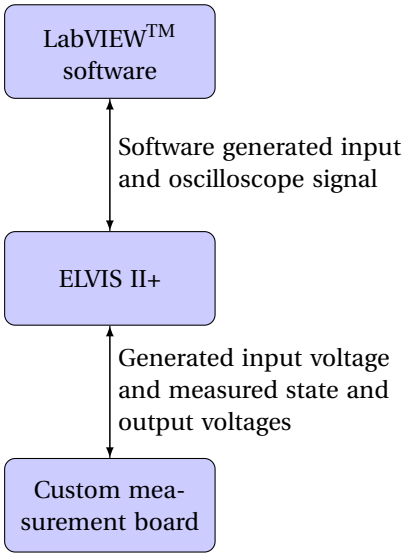


Figure 6: Block diagram showing the components of the assembled measurement framework and their interconnections.

work layout for this topology.

A third general circuit design is proposed (Figure 8a), which can be implemented as a $2 \times 2 \times 4$, three dimensional grid structure on a multilayer carrier. This new circuit has a better compromise between open and short connection faults, but can only be constructed effectively in a three dimensional structure. The disadvantage is that since the height of the grid is even, and the top and bottom electrodes are aligned, they cannot form a crossbar network.

A workaround could be that this type of network can scale with the height of the 2×2 column, and it can be $2 \times 2 \times 3$ or $2 \times 2 \times 5$ sized. These new non-general networks result in different memristor parameters. The advantage of an odd height is that it can be realized in a crossbar network, as can be seen in Figure 8b.

Another important property to consider is the chip area used. These networks should be implemented efficiently on a chip as a two dimensional crossbar network. The implementation of the previous networks was only possible using sixteen times more chip area for the emulation of a single device. The new network uses more vertical layers, but only 4 times more area

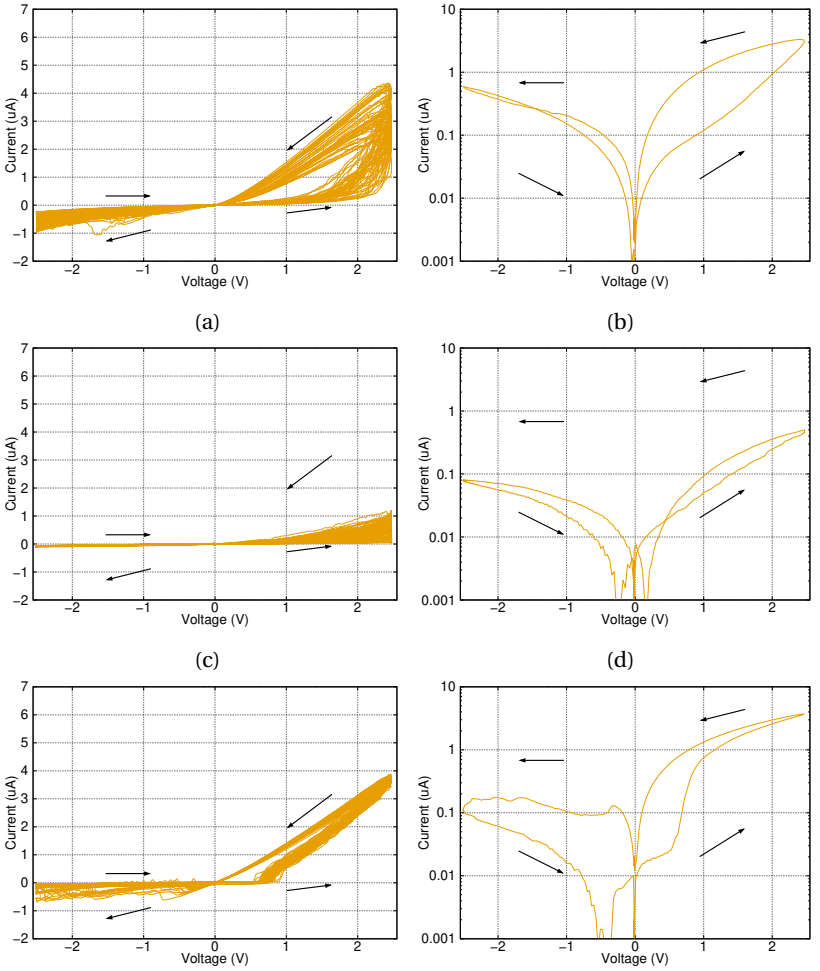
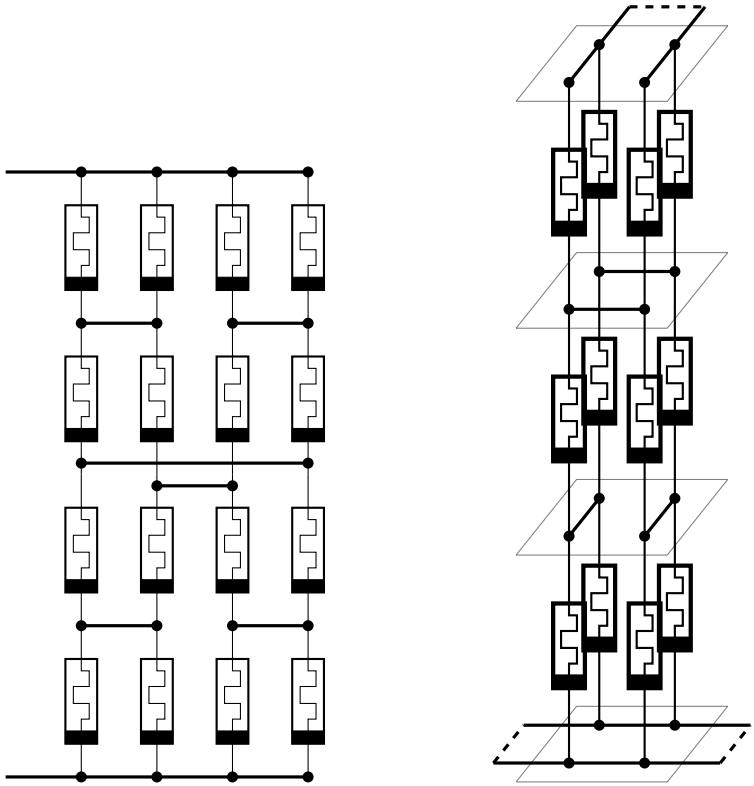


Figure 7: Short-time pulses on a single memristor, the checkerboard like and the H-fractal memristor network, respectively. (**a**), (**c**) and (**e**) show the Voltage-Current diagram of the whole signal. (**b**), (**d**), (**f**) are the average of the absolute value of all 50 write-erase signals on a logarithmic scale.

with a similar reliability gain, as compared to a single memristor. The result can be seen in Table 2



(a) (b)

Figure 8: The memristor arrays designed by me. I validated by measurements that these new type of networks are more robust than the previously presented networks. Design (a) is similar to the earlier versions and consists of 16 memristors, while layout (b) contains only 12 elements, allowing it to be efficiently arranged in three dimensions.

Publications supporting Thesis group II.: [J1,C3].

Thesis group III.

3. I designed and implemented a new Memristor Cellular Neural Network (MCNN) template that enables the implementation of the XOR logic opera-

Table 2: The table shows the main properties of emulating memristor networks. The best values are indicated, namely the highest high-resistance state (HRS), the lowest low-resistance state (LRS), the largest HRS/LRS ratio. Lower dispersion is also considered better.

Measured object	OFF resistance	ON resistance	ON/OFF ratio	Dispersion Index
Single memristor	5.7889 MΩ	0.7185 MΩ	8.0569	0.04553
H-fractal network	19.472 MΩ	0.6717 MΩ	28.990	0.02718
Checkerboard network	20.322 MΩ	5.4633 MΩ	3.7197	0.04921
3D 2x2x4 network	**20.651 MΩ**	0.7072 MΩ	**29.201**	**0.01800**
3D 2x2x3 network	9.3426 MΩ	**0.4194 MΩ**	22.276	0.02491

tion within a single cell.

3.1 I improved the two-variable Dynamic Route Mapping (DRM2) visualization tool to use saturated colors and three-dimensional surfaces to support the design of new MCNN templates.

Memristor Cellular Neural Networks (MCNNs) are a promising approach for neuromorphic computing, but they lack of new templates and studies that demonstrate significant improvements over classical Cellular Neural Networks (CNNs). One of the main reasons for this is the complexity of their underlying mechanisms, which involve the nonlinear behavior of memristors. As a result, there is still a need for more research to show clear benefits of MCNNs compared to traditional CNN architectures.

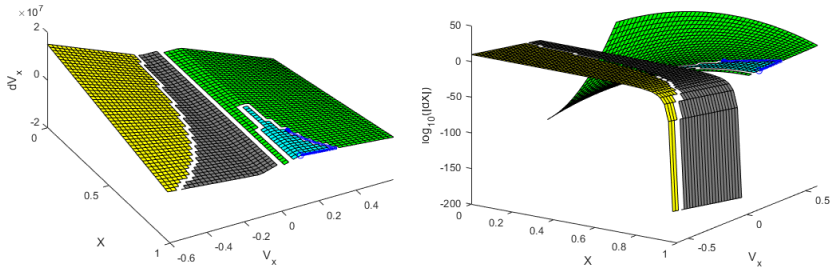
To address this, improved visualization methods could be helpful in making the inner workings of MCNNs easier to understand. Clearer visual representations of how memristor-based networks operate could give researchers and developers a better understanding of their unique features. This could lead to the design of more effective MCNN templates and provide a stronger basis for comparing their performance with classical CNNs.

The simulations in this section used a TaO_x memristor model. Here I present 2 new types of the existing [14] DRM_2 visualisation tool. In these visualizations, x and v_x denote the memristor state and the voltage of the MCNN cell capacitor, respectively, while $\dot{x}$ and $\dot{v}_x$ represent their derivatives. The colored surfaces illustrate the states accessible to the cell, and the colors vary according to the state derivatives as follows:

Green region (I):	$\dot{x} < 0 \cap \dot{v}_x < 0$
Cyan region (II):	$\dot{x} < 0 \cap \dot{v}_x > 0$
Gray region (III):	$\dot{x} > 0 \cap \dot{v}_x < 0$
Yellow region (IV):	$\dot{x} > 0 \cap \dot{v}_x > 0$
Red cross:	$\dot{x} = 0 \cap \dot{v}_x \neq 0$
Purple rhombus:	$\dot{x} \neq 0 \cap \dot{v}_x = 0$
Unfilled black circle:	$\dot{x} = 0 \cap \dot{v}_x = 0$, and unstable equilibrium
Filled black circle:	$\dot{x} = 0 \cap \dot{v}_x = 0$, and stable equilibrium
Blue line:	Second-order State Dynamic Routes (SDR_2)

The first (Figure 9) new version is a more straightforward one, showing the derivatives of the two states on the Z-axis. This 3D representation provided some insight on how an MCNN cell evolve in time and prompted the following saturated color visualisation.

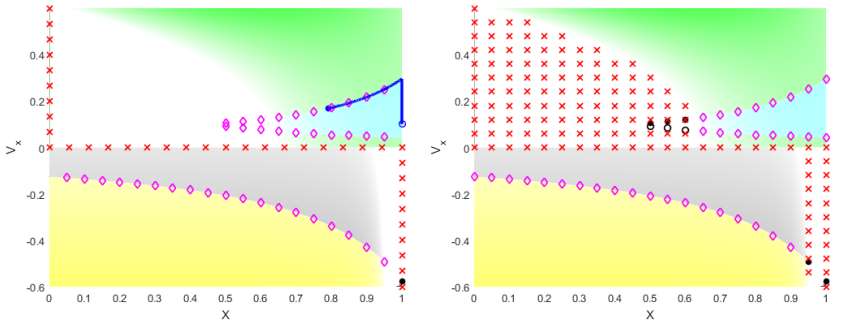
The saturated color map (Figure 10) is created for the memristor state evolution, is based on the following rules. The color is following the memristor state derivative from 10^7 to 10^{-20} logarithmically. The zero saturation (full color) means that the memristor dynamics is significantly faster, than the capacitor change, while the high color saturation (lighter color) means that the memristor dynamics is significantly slower, than the capacitor change. White colored region can be considered a stable for the memristor dynamics in a constrained timeframe. Note that such values are roughly 26 orders of magnitude smaller than cell state derivatives and - according to the TaO_x model - would require several years to make noticeable difference on the graph.



(a) DRM2 with the cell state derivative on the Z-axis. The scale is linear and the average order of magnitude of the derivative is 6.

(b) DRM2 with the memristor state derivative on the Z-axis. The scale is logarithmic and the order of magnitude of the derivative ranges from -100 to 10.

Figure 9: The 3D visualization designed by me.



(a) White color indicates very small derivatives. The blue line represent an example MCNN cell state evolution

(b) DRM2 with indications about the type of stability for color saturated regions.

Figure 10: Saturated color DRM2 designed by me.

3.2 Using the visualization tool, I designed a new MCNN template, the XOR template, which implements the logical XOR operation within a single MCNN cell.

The two state derivatives evolve in a fundamentally different way. While the capacitor voltage change linearly, the memristor state change is exponential. Therefore in certain regions of the DRM_2 only the voltage changes while in other regions only the memristor state changes and its only a narrow, intermediate band between the two, where both states varies significantly.

Exploiting this realization, it seems reasonable to design with these regions independently from each other. More specifically, with a certain parameter set, the memristor state can act as a switch between 2 fundamentally different regular CNN macro state. When the memristor is in a low resistance state (LRS), the MCNN cell behave as a monostable CNN cell would, while the memristor is in high resistance state (HRS), the MCNN cell is bistable (Figure 11).

It seemed logical to use the memristor state as one of the XOR inputs, leaving only the values of the other input to be determined. The required parameters can be seen on Table 3. Here, u denotes the input of the MCNN cell, while $v_{x_{init}}$ represents the initial voltage of the MCNN cell capacitor. The variable x_{init} varies between 0 and 1 and represents the initial state of

the memristor.

A	B	XOR
$u = 0.1$ & $v_{x_{init}} = -0.1$	$x_{init} = 0$	0
$u = 0.1$ & $v_{x_{init}} = -0.1$	$x_{init} = 1$	1
$u = -0.1$ & $v_{x_{init}} = 0.1$	$x_{init} = 0$	1
$u = -0.1$ & $v_{x_{init}} = 0.1$	$x_{init} = 1$	0

Table 3: Implementation of the XOR operation.

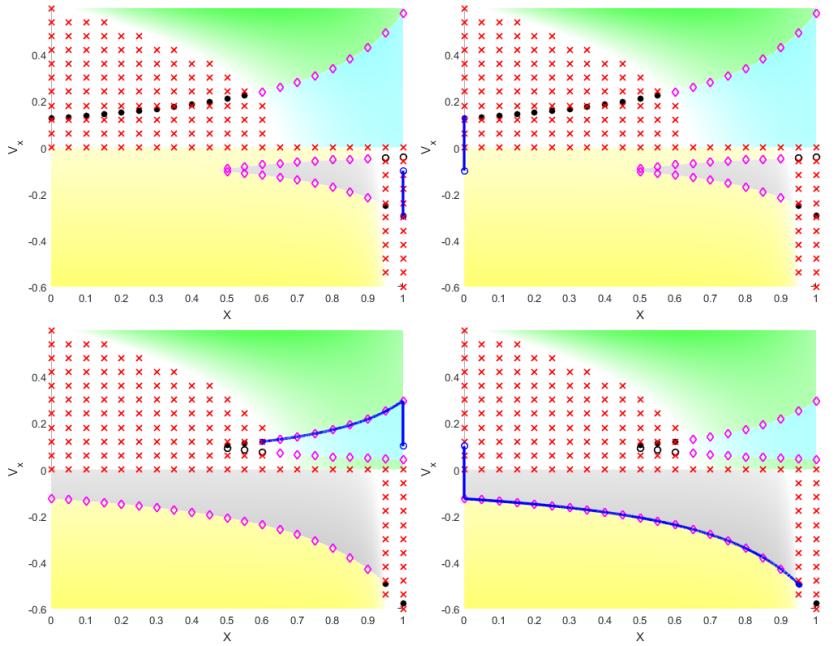


Figure 11: The four cases of the XOR boolean operation. The empty blue circle and the filled blue circle marks the starting state and the final state of the dynamics, respectively.These determine the direction of the trajectory represented by the continuous blue line.

3.3 I designed and implemented an isolated Memristor Cellular Neural Network (MCNN) cell circuit and then verified the implementation by realizing and measuring the MCNN-specific STORE *and* RECALL *templates.*

The circuit design is shown on Figure 12. It is inspired by the CNN cell circuit implementation [15]. Op amp O_1A and resistors $R_1 - R_3$ computes the weighted sum of analogue voltages. Op amp O_1B with resistors $R_4 - R_7$ and potentiometer P_1 implement an improved Howland Voltage Controlled Current Source (VCCS). Op amp O_2A with resistor R_9 and potentiometer P_2 realizes an approximation of the piecewise-linear standard non-linearity function. Buffer capacitor C_b filters out the high frequency noise components from the output signal v_{out}, ensuring a safe operation for the feedback

branch. C_b operates only on the output stage, and thus does not increase the number of degrees of freedom of the memcomputing core. R_8 is used in series with the memristor to limit the current across the memristor device and provides a point of indirect measurement at the node at voltage v_{meas}. The gray box is a relay, controlled by the voltage V_C, falling across a coil, and setting the initial values of the MCNN states, i.e. the voltage v_x across capacitor C, and the memristor state x. The relay has no effect during the MCNN operation.

The operation of the STORE and RECALL templates is closely related to the memristor element of the MCNN cell. As their names suggest, the purpose of the STORE template is to store a binary value given at the cell's input in the memristor unit in the form of a low or high resistance state. The purpose of the RECALL template is to read the binary value stored in the memristor and display it at the cell's output in the form of a positive or negative saturation voltage level.

Figure 13 show examples with simulation and measurement results.

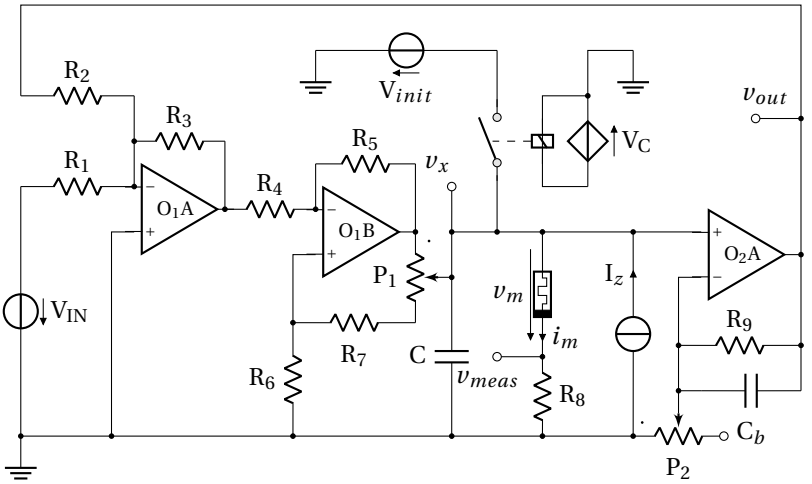
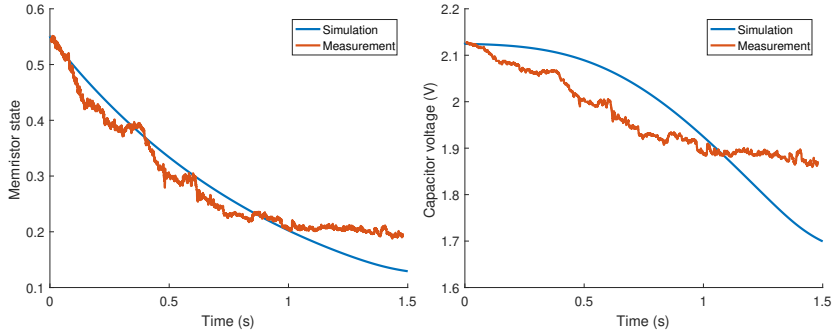


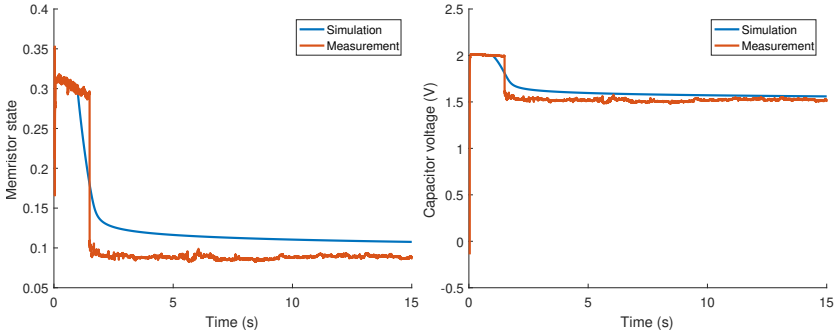
Figure 12: Novel implementation of the isolated MCNN cell circuit.

3.4 I implemented the designed template on the isolated MCNN cell circuit and verified the XOR template simulation results through measurements.

In the context of this experiment, the XOR operation is defined as follows. $Input_A$ is the memristance of the memristor, can be either LRS or HRS,



(a) Memristor state and capacitor voltage change in the case of the STORE template.



(b) Memristor state and capacitor voltage change in the case of the RECALL template.

Figure 13: STORE and RECALL template measurement comparison of state variables with simulation results.

while $Input_B$ is both the MCNN cell input and MCNN cell capacitor voltage. The $Output$ is the sign of the MCNN cell output.

Figure 14 shows the summary of the measurement. The state initialization and demonstration of the four cases of XOR is starting at $t = 0s$, $t = 1s$, $t = 2s$ and $t = 3s$.

Publications supporting Thesis group III.: [C4,C5,C6].

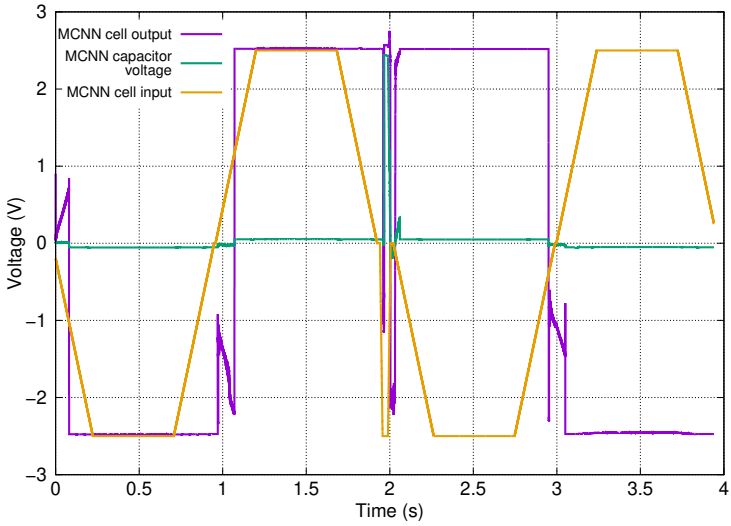


Figure 14: Summary result of the measurement. For the first and second case the output follows the sign of the MCNN cell input and after a memristor state erase signal the output follows the inverse of the sign of the MCNN cell input. During operation the MCNN cell capacitor voltage is kept small to avoid unwanted memristor state change.

4 Areas of application

In thesis point 1, the measured memristor characteristics are essential for understanding and accurately modeling memristor behavior. By mapping the relationship between resistance and voltage, I characterized the nonlinear features of memristor behavior, which play a key role in controlling the writing, reading, and erasing of memory states. This information enables the development of models that accurately describe how the memristor state changes in response to applied electrical signals, thereby facilitating the development of more reliable and efficient devices.

In thesis point 2, the implemented memristor networks play a significant role in creating more stable devices by enabling the production of a single, more reliable emulated memristor through the combined use of multiple memristors. Measurements indicate that the cycle-to-cycle variations in the networks are smaller than those of individual memristors, resulting in lower variance. Consequently, memristors organized into networks can contribute

to the development of more stable and predictable devices, which is particularly important for industrial manufacturing and applications.

In thesis point 3, the visualization tool utilizing saturated colors and 3D surfaces enables the development and fine-tuning of MCNN templates, such as the XOR template, which can perform complex logical operations within a single cell. The implementation of the isolated MCNN cell circuit and the successful testing and measurement of the templates demonstrate that the MCNN platform is stable and effective. Based on these results, the MCNN is suitable for implementing new image processing algorithms.

Journal publications of the author

[J1] **Dániel Hajtó**, Ádám Rák, György Cserey "Robust Memristor Networks for Neuromorphic Computation Applications," *Materials*, vol. 12, no. 21, pp. 3573, 2019.

[J2] **Dániel Hajtó**, Waleed El-Geresy, Deniz Gündüz, György Cserey "State Characterisation of Self-Directed Channel Memristive Devices," *Engineering Research Express*, accepted manuscript, 2025.

Conference publications of the author

[C1] **Hajtó Dániel**, Cserey György "SPICE model for CMOS based memristor implementation," *2018 21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (IEEE DDECS)*, 2018.

[C2] **Hajtó Dániel**, Cserey György "Multistate-switching based memristor modeling in a Python based SPICE-like circuit simulator," *PhD Proceedings Annual Issues of the ROSKA Tamás Doctoral School of Sciences and Technology, Faculty of Information Technology and Bionics, Pázmány Péter Catholic University*, vol. 1, no. 1, pp. 34, 2019.

[C3] **Hajtó Dániel**, Cserey György "Emulation of a single fault-tolerant memristor with memristor networks," *PhD Proceedings Annual Issues of the ROSKA Tamás Doctoral School of Sciences and Technology, Faculty of Information Technology and Bionics, Pázmány Péter Catholic University*, vol. 1, no. 1, pp. 45, 2020.

[C4] **Hajtó Dániel**, Cserey György "Developing a measurement environment for the Memristor Cellular Neural Network architecture," *PhD Proceedings*

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[C6] Paolo Dini, **Hajtó Dániel**, El-Geresy Waleed, Tolga M. Duman, Deniz Gunduz, Cserey György "SONATA - sustainable computing and communication at the edge 2023," *CHIST-ERA 2023 Project Seminar, Bratislava*, 2023.

[C7] Paolo Dini, **Hajtó Dániel**, El-Geresy Waleed, Tolga M. Duman, Deniz Gunduz, Cserey György "SONATA - sustainable computing and communication at the edge 2024," *CHIST-ERA 2024 Project Seminar, Helsinki*, 2024.

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[C9] El-Geresy Waleed, **Hajtó Dániel**, Cserey György, Deniz Gunduz "Energy-Information Trade-Off in Self-Directed Channel Memristors," *IEEE International Workshop on Machine Learning for Signal Processing (IEEE MLSP)*, 2025.

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[O1] Badics Tamás, **Hajtó Dániel**, Tornai Kálmán, Kiss Levente, Reguly István Zoltán, Pesti István, Sváb Péter, Cserey György "Integral representation method based efficient rule optimizing framework for anti-money laundering," *Journal of Money Laundering Control*, vol. 26, no. 2, pp. 290–308, 2023.

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