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BRAIN ACTIVITY MEASUREMENT WITH IMPLANTABLE MICROCHIP

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A thesis submitted for the Doctor of Philosophy

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Alul írott Dr. Földesy Péter Témavezető nyilatkozom, hogy *Kárász Zoltán* doktorjelölt publikációs teljesítménye megfelel a doktori (PhD) fokozatszerzési eljárás előfeltételeként a Tudományterületi Doktori és Habilitációs Tanács által támasztott követelményeknek.

2. PhD disszertáció

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Dr. Földesy Péter, PhD, Egyetemi docens

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GLOSSARY OF TERMS

ALS – Amyotrophic Lateral Sclerosis disease

AP – Action Potential

CMFB - Common Mode Feedback

CPA – Constant Phase Angle

DNEF – Distortion supplemented Noise Efficiency Factor

EEG - Electroencephalogram

FMRI - Functional magnetic resonance imaging

KF – Flicker Noise Coefficient

LFP – Local Field Potential

LNA – Low Noise Amplifier

MEA – Multi Electrode Array

MUA – Multi Unit Activity

OTA – Operational Transconductance Amplifier

NEF – Noise Efficiency Factor

PMMA – Poly Methyl Methacrylate

THD – Total Harmonic Distortion

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I. INTRODUCTION

The biomedical field is one of the most dynamically developing research area in the analog IC design, especially those concerning low-power implementation including implantable without battery. The examination procedures need more time for the functional result than available using other observing techniques as the FMRI or using simple EEG [1, 2]. Even though the portability of the measuring instrument is not an important issue for the animal studies, it is in the human experiments.

In the following it will be presented in-vivo techniques currently used for brain activity recording in electrical engineering point of view. Like most of the engineering task we need to make compromises to get a solution which meets the initial specification. We have to understand what type of environment where the chip will be integrated. In our case where the main object to record electrical signals in the central nervous system it is necessary to know what types of signal are we going to measure. Like what are the expected signal levels, frequencies or allowed noise levels. How the signal will be distorted by the tissue or the electrode itself and how it will be aging. This work starts with a biomedical introduction that helps to understand what parameters we have to keep and what we can neglect. The current solutions in literature do not deal with the low frequency distortion, based on the idea that information can be ignored. In this work I will show the most widely accepted solutions then introduce a new architecture which helps to optimize the noise and distortion levels at low frequencies.

Our interest concerts indeed the implantable cortical micro sensor arrays, which causes minimal structural damages in the analyzed region. From the engineer's aspect measuring the brain activity could be simplified to an electrical connection between the brain tissue and the electrode. The implantable neural recording devices have to achieve strict specifications, including the power consumption, noise and distortion requirements, defined maximal thermal dissipation and specified input frequency range.

The very basic motivation to do research in this field because it's easy to where can we use our results. In short term the better electrophysiological recording can helps to understand brain functions. In longer term can helps on those patients who suffer some loss in motoric functions while the cognition is still intact.

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Possible cause:

- Spinal cord injuries
- Stroke
- Parkinson's disease
- Cerebral palsy
- Muscular dystrophy
- Amyotrophic lateral sclerosis or Lou Gehrig's disease
- Limb loss

Neural Recording

A. Background

The neuron is the basic unit for processing information in the human brain. Early in the last century scientists realized that most neurons transmit information by generating electronic pulses called spikes or action potentials. More and more researchers have investigated the correlation between neuron spiking activity and associated subject behavior. Furthermore, some research groups have used the recorded spikes trains of many neurons to generate real-time commands for controlling mechanical interfaces [3] or stimulating peripheral nervous systems [4], leading to the growing field of brain machine interfaces. Simultaneous detection of signals from many neuronal cells is necessary [3], in order to understand the mechanisms of information processing in the correlated activity of different neurons and subsequent applications. The recording of the neural signals from the central nervous system is typically performed using recording micro- electrodes that are intrusively implanted into the relevant parts of the brain. A great deal of effort has been expended during the past few decades on the development of suitable recording instrumentation tools to allow long-term, stable and high-quality recording. The research proposed herein addresses the IC hardware realization of ultra-low power neural recording systems using novel pulse representations. An irony of this research is that the pulse

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signal representations used to encode the recorded signals were inspired by the spiking neurons themselves.

B. Extracellular signal

The neural signal most widely recorded is the extracellular bio-potential generated electrochemically by individual neurons. When a neuron receives sufficient stimuli from other cells, its cell membrane depolarizes, causing ionic currents to flow in its extracellular space. Consequently, an extracellular signal is generated from the electrical charge imbalance (among Na, K, Cl and other ions) near the outside of the biological membrane. The voltage drop associated with this extracellular single-unit action potential is a spike of about 50-500 μV in amplitude, with frequency content from 100 Hz to about 10 kHz [5]. Normally, action potential waveforms are either bi-phasic or tri-phasic; pulse widths are typically 1-1.5 ms [6]. The noise floor, which includes biological noise from far field neurons and thermal noise from electrodes could be as high as 20 μV_{rms}. Due to the unavoidable electrochemical effects at the electrode-tissue interface, DC offsets ranging from 0.1-0.5 V across the recording sites. Besides neuronal spikes, researchers are also interested in activities of large groups of neurons. The synchronous firing of many neurons near the electrode results in a low frequency oscillation, which is called the Local Field Potential (LFP). Previous research has shown that the energy of the LFP in primate pre-motor and motor cortex correlates with specific arm reach movement parameters [7]. The frequency range of the LFP is less than 100 Hz normally and could extend down to less than 0.1 Hz.

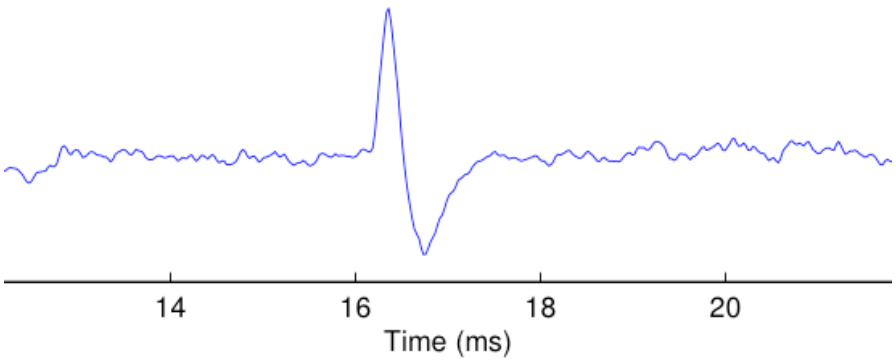

Fig. 1.1 Typical neural signal [8]

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C. Electrodes

The electrophysiological recordings can be classified by the types of recording:

- Intracellular (Patch-clamp electrode)
- Extracellular
- Surface
- Epidural
- Scalp (EEG)

Each types have unique values and difficulties. While the patch-clamp measurement gives the most details it can be used only in vitro environment. Unfortunately, the neural signals are degrading when we try to record through more and more tissue. It means lower resolution and less detail.

To make a good characterization it is necessary to understand the important parameters. How they alter the received signal. The basic electrode parameters:

- Impedance
- Potential
- Stability (biocompatibility)
- Aging

The stability and aging are connected. It means when and electrode or integrated circuit are implanted it is needed to make sure we minimize the biological effects, like inflammation or encapsulation which increase the resistance among the tissue and electrode. We have to calculate with electrical effects between the tissue and the probe:

- Resistance lower output signal amplitude
- Capacitance reduced high frequency
- Double layer effect on metal-fluid contact

To able to understand what is happening inside the cell at first we need build an electrical model for the electrode tissue connection.

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D. Electrode models:

a) The first published electrode model made by Warburg in 1899.

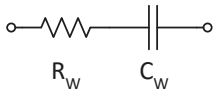

Fig. 1.2 Warburg's electrode model

$$R_W = \frac{1}{k\sqrt{\square}} \qquad C_W = \frac{k}{\square} \qquad \square = \frac{\square}{4} \tag{1.1}$$

$$R_W = \frac{1}{k\ \square} \qquad C_W = \frac{k}{\sqrt{\square}} \qquad \square = \frac{\square}{4} \tag{1.2}$$

$$C_W = \frac{k}{\square} \qquad \square = \frac{\square}{4} \tag{1.3}$$

b) Randle (1947) /rapid model/ – It introduced the C_p double-layer polarization capacitance

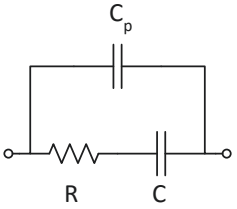

Fig 1.3 Schematic of the rapid model

c) Sluyters

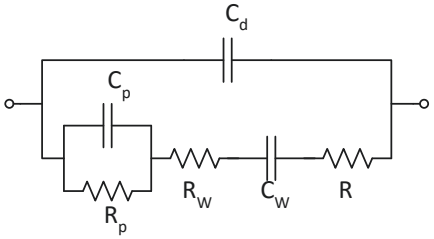

Fig 1.4. Sluyter's electrode model

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d) Gregor Kovacs – It firstly included a possible DC current path

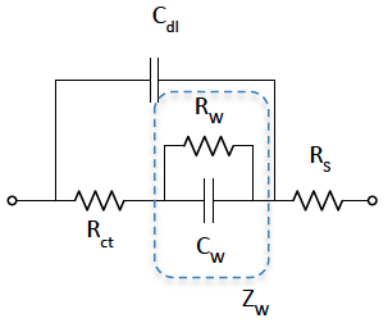

Fig. 1.5 Schematic the Kovacs's model

C_{dl} double layer capacitance

R_{ct} charge transfer resistance

$$Z_W = \frac{(1-j)}{k\sqrt{\omega}} \tag{1.4}$$

e) Hierlemann (2005) – The double layer effect was implemented as CPA. This is the most often use model since.

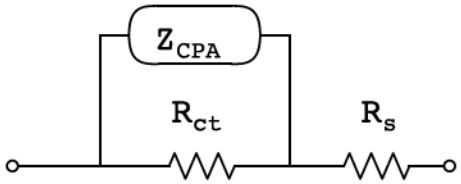

Fig. 1.6 Hierlemann model

$$Z_{CPA}(\omega) = \frac{1}{(j\omega Q)^n} \tag{1.5}$$

CPA – constant phase angle

$Z_{CPA} \approx C_{DL}$

- Q measured magnitude (impedance)

- n constant representing the inhomogeneity of in the surface ($0 <= n <= 1$)

(if n = 1 the ZCPA purely capacitive impedance element)

- $\omega = 2\pi f$

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$$\frac{1}{C_I} = \frac{d_{OHP}}{\varepsilon_0 \varepsilon_r} + \frac{L_D}{\varepsilon_0 \varepsilon_r \cosh\left(\frac{z\phi_0}{2U_t}\right)} \tag{1.6}$$

Interface capacitance:
- d_{OHP} thickness of double layer
- ε_0 is the permittivity of the vacuum
- ε_r is the permittivity of the double layer
- z is the charge of the ion
- ϕ_0 electrode potential
- U_t thermal voltage

$$L_D = \sqrt{\frac{\varepsilon_0 \varepsilon_r U_t}{2n^0 z^2 q}} \tag{1.7}$$

Debey length:
- n^0 bulk number concentration in solution
- q is elementary charge

$$R_s = \frac{\rho}{4r} \tag{1.8}$$

Solution resistance (spreading resistance):

- ρ is the solution resistivity (72 Ωcm for physiological saline)
- r radius

$$R_t = \frac{U_t}{J_0 z} \tag{1.9}$$

R_t – charge transfer resistance (highly depend about the initial electrode-electrolyte conditions)

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$$U_t = \frac{kT}{q} \approx 0.0259V \tag{1.10}$$

Parameter	Pt	TiN
R_S [Ω]	28	83.8
R_{ct} [Ω]	42.3	$3e^5$
Q [$s\Omega^{-1/n}$]	$2.72e^{-5}$	$2.03e^{-3}$
n	0.92	0.91
C_I [F/m^2]	0.545	
Z_{CPA} [Ω]	$1.59e^4$	

Table 1.1 Resistance and capacitance values for platina and titanium nitride material

Parameter	Pt
d_{OHP}	5 Å
ε_0	$8.85e^{12}$ F/m
ε_r	78
z	4
U_t	0.0259 V
n^0	$9.3e^{25}$ ions/m^3
q	$1.602e^{-19}$ C

Table 1.2 Typical detailed values for the platina electrode

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f) Martin (2008) – designed for nanotube construction

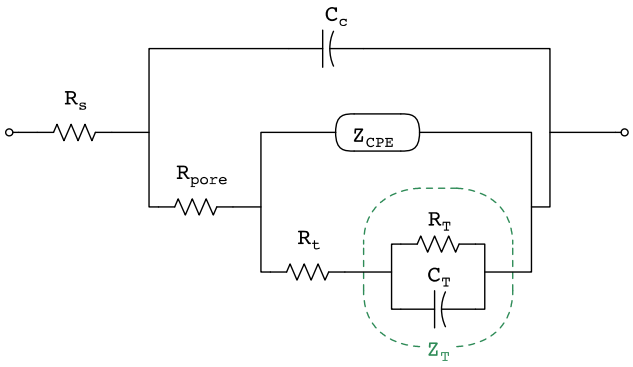

Fig. 1.7 Schematic for the Martin nanotube model

R_s – solution resistance

C_c – coating capacitance

R_{pore} – pore resistance

Z_{CPE} – double layer impedance

R_t – charge transfer resistance

Z_T – finite diffusion impedance

MEA	Sites (MEAs) surveyed	Mean Qcap [mC/cm^2]	Mean $Z_{1\ kHz}$ [kΩ]	Funct. sites [%]
Cyberkinetics Iridium Oxide Array	64 (4)	10.4	74.1	93.8
Cyberkinetics Utah array	96 (3)	6.10	194	90.6
Moxon Ceramic Array	12 (3)	1.4	184	100
NeuroNexus Silicon Array	64 (4)	0.8	270	95.3
Tucker-Davis Microwire Array	48 (3)	5.1	19.9	100

Table 1.3 parameters of the purchasable electrode arrays

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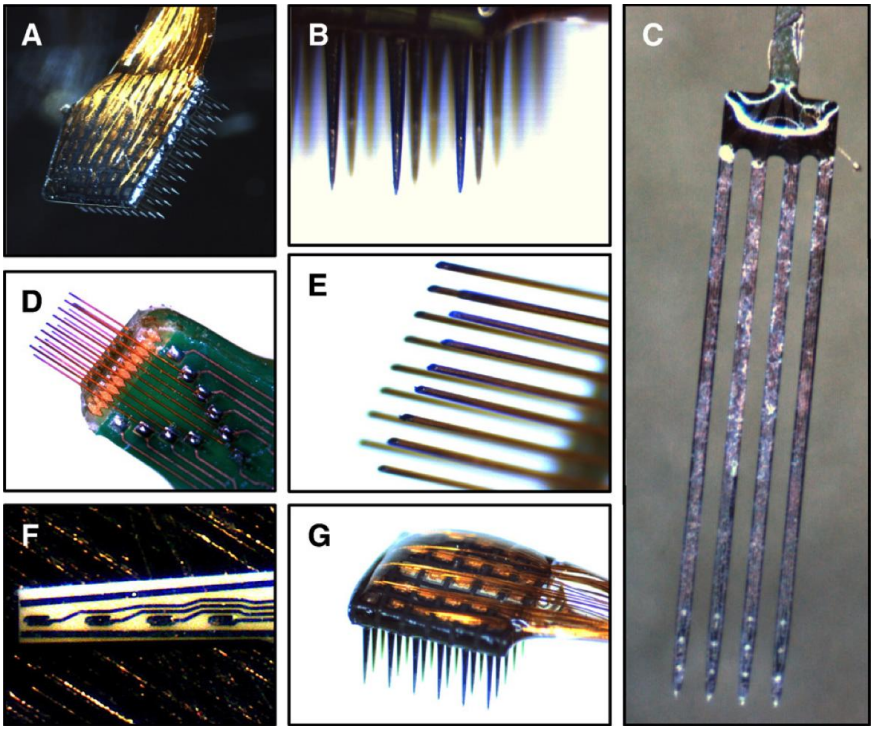

Fig. 1.8 Example multi electrode arrays

(A) Cyberkinetics Silicon-based 100-channel MEA.

(B) View of recordings sites on the Cyberkinetics arrays (metallic portion on tip of each shank).

(C) View of NeuroNexus Silicon-based MEA shanks (4 linearly spaced recording sites are seen on each of the 4 shank tips).

(D) Tucker-Davis Technologies Microwire MEA.

(E) View of recording sites on the TDT microwire array (sites were cut at 45°).

(F) Moxon Thin-Film Ceramic-based MEA (Moxon et al., 2004a; Moxon et al., 2004b) (Top: base of shank, Bottom:

(G) View of bond pads on a 36-channel Cyberkinetics array.

The electrodes are the first and the most critical stage of hardware for neural recording. Electrode properties impact both the effectiveness of the initial recording and the performance of the subsequent amplification circuitry. In order to record the action potentials, the electrodes must be small enough to penetrate the clefts between cells and approach active neurons without damaging them. Hence, the size of the electrodes should be comparable to neurons (normally 50 μm or less) and the tips of the electrodes

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should be sharp enough to penetrate neural tissues. In addition to the physical requirements, there are also biological, chemical, mechanical and electrical constraints that the recording electrodes must satisfy. Ultimately, the recording sites should be stable against long-term exposure to biological fluids and must be capable of recording the electrical signals with minimum noise.

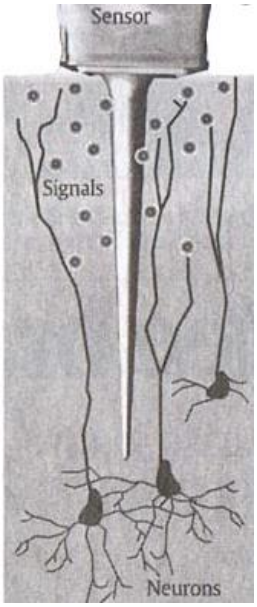

Fig. 1.9 Extracellular electrode

E. Passive electrode types:

A passive electrode is defined does not contain any interfacing electronic circuitry on the electrode substrate [9]. Three basic types of passive electrodes are used by neurophysiologists: metal, glass-micropipette and photoengraved microelectrodes.

Metal micro-wires consist of a wire sharpened to provide a tip small enough for cellular study. The materials chosen for this application include platinum, gold and stainless steel. The surfaces are isolated with Teflon or polyimide [10]. The wires are usually cut to length with sharp surgical scissors, exposing a single recording surface per wire (typically 1 to 100 μm2). Metal microelectrodes are most suitable for extracellular recording situations where neural discharges have a medium to high frequency content. The electrochemical potentials developed across this interface are sensitive functions of the electrode surface properties and of the ionic concentrations near that surface. These DC potentials are normally many times larger than the extracellular potentials and slowly drift in time masking any AC extracellular

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bio-potential generated by neurons. Consequently, designers must be careful that the large DC component will not saturate the signal acquisition system.

The **glass micropipette** electrode is made from a 1-2 mm diameter glass tube which is heated and drawn down until it is pulled in two [11]. By controlling the temperature and applying a force on the tube, the wall thickness and shank taper can be satisfactorily controlled. The resulting tip diameter generally ranges from 1 μm down to 0.1 μm. These electrodes contact the neurons through the fluid junction at the tip of the pipette, where the charge carriers are ions. When there is a difference between the concentrations or compositions of the cellular and pipette electrolytes, a steady junction potential is set up across the liquid interface. The sum of this potential and the potential of the reversible Ag/AgCl electrode in the pipette stem relative to the reference electrode can be measured. These potentials are constant and do not vary as the electrode is advanced. Therefore, pipettes can be used to measure DC and low frequency bio-potentials and can provide some information about the Local Field Potential (LFP). Although this type of electrode avoids the isolation problems associated with metal electrodes, they are limited in useful bandwidth to a few kHz and are susceptible to tip breakage [11].

The **photoengraved microelectrode** is complex electrode design allows the capability for integrating electronics and cabling. They are fabricated using technologies developed for silicon integrated circuits. These microelectrodes are fabricated by depositing and patterning thin film electrodes on a thick substrate, which acts as the carrier. The electrodes are insulated on top and bottom by thin-film dielectrics. Recording sites are defined and etched through the top dielectric, and the finished microelectrode is separated from the host substrate. Substrate materials used for these microelectrodes include silicon, tungsten, molybdenum, glass and polyimide. The thin film dielectrics used have included polyimide, silicon oxide, silicon nitride, PMMA and glass. The electrode conductor has been made with gold, platinum, tungsten, tantalum, and nickel [12]. One of the advantages of this type of electrode is the possibility of multiple recording sites per electrode. [13]. In order to provide an optimal implant environment and extend the longevity of the tissue-electrode interface, the flexibility and bioactivity of the electrodes should be considered. There are some polyimide-based electrodes designed for the curved surface of the brain. The forces of “micro-motion” between the tissue and the implanted device can be relieved because of the flexibility of the polyimide. Furthermore, the chemical properties

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of the polyimide surface allow a host of bioactive organic species to be either adsorbed or covalently bonded to its surface [14]. A prototype polyimide flexible electrode array for implantable neural recording is proposed in [15]. The gold-plated nickel electrodes with parylene-C insulated shanks are placed on the flexible polyimide ribbon cable. Not only can this design provide multiple recording sites on one cable, but also the flexible cable can be 'bowed' for strain relief on the implant.

One of the major challenges in interfacing electronics to a recording electrode is the random wandering of the voltage associated with the electrochemical, metal-electrolyte interface. The DC potential between an electrolyte and a metal electrode is subject to substantial variations and can be as high as 50 mV for a gold surface, which is 1000 times the action potential at the recording site. The optimal front end suppresses the DC shift while keeping decent AC gain.

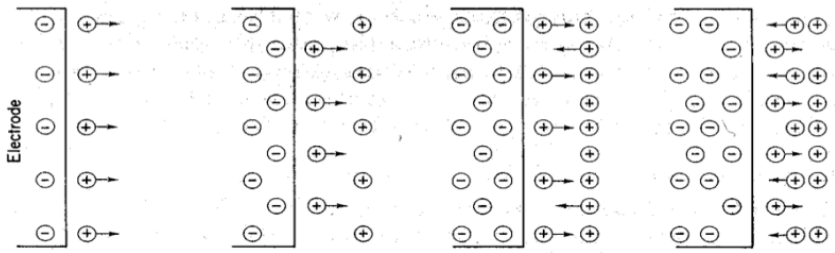

Fig. 1.10 Double layer effect on metal-electrolyte interface

F. Amplifier Requirements

The realization of large time constants is fundamental for design filters with very low cut-off frequencies especially in implantable biomedical sensors. The filters are required to be tunable. In addition, realizations with low power dissipation and small size are also critical. Several approaches for the design of integrators with very large time constants have been reported [16-17]. The trivial solution to employ on-chip physical resistor and capacitor requires large chip area and it would not be tunable. The possible solutions can be categorized into pseudo-resistor implementations [3,5,16,17], switched-capacitor (SC) methods [15-17] and operational trans-conductance amplifier capacitor (OTA-C) techniques with very small trans-conductance's [15-17] to allow the on-chip capacitance to be kept manageable low.

Possible methods to implement large time constant:

- On-chip physical resistor
- *MOS pseudo-resistor*
- Switched capacitor resistor
- OTA with small transconductances
    - Capacitance scaling
    - Current division
    - Current cancellation

G. MOS Pseudo-Resistor

This work is based on pseudo-resistors, as they outperform other solutions in term of power and area efficiency to reach large time constant. The pseudo-resistance has good size and parasitic values (in the range of fF), but it also has some serious non-ideal behavior, which means poor robustness and bad distortion in the LFP range. In the next chapter I will introduce a new architecture in order to avoid the low frequency signal distortion and explain the compensation method in details.

To able to handle the pseudo element it is necessary to modeling the resistance of the MOS transistor.

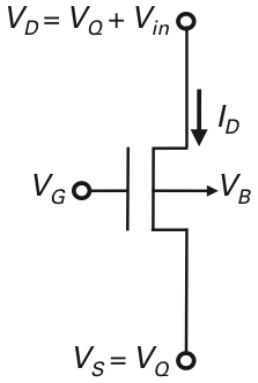

Fig. 1.11 Transistor model

A descriptive linear model bases on the following components [6]: the source diffusion; the channel resistance; accumulation resistance; component resistance; drift region resistance; substrate resistance. For more appropriate result it is needed a nonlinear approximation.

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$$\frac{1}{R}\Big|_{V_{DS}=0} = \frac{dI_D}{dU_D}\Big|_{V_{DS}=0} = -\frac{dI_D}{dU_S}\Big|_{V_{DS}=0} = g_m = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_f}-1\right) \tag{1.11}$$

In the strong inversion and weak inversion region it is possible to explain the resistance as following:

$$\frac{1}{R}\Big|_{V_{DS}=0} = g_m = \mu C_{ox}\frac{W}{L}\left(V_G - V_{T_0} - nV_Q\right) \tag{1.12}$$

$$g_m = \frac{2I_S}{\phi_t}\left(\frac{1}{2}i_f\right) = \frac{2I_S}{\phi_t}exp\left(\frac{V_G - V_{T_0} - nV_Q + n\phi_t}{n\phi_t}\right) \tag{1.13}$$

where n is the slope parameter.

The most prevalent utilization of the MOS transistor as a resistor is the pseudo-resistor. That is construing the features of this solution, like the minimal size, simplicity and the outstanding effective resistance [18].

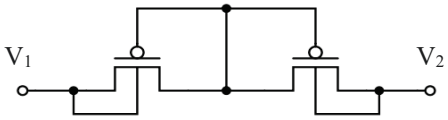

Fig. 1.12 Schematic of the pseudo-resistor element

The basic symmetric element contains two transistors that are connected as a MOS diode and a parasitic source-bulk diode connected in anti-parallel. If the voltage across the device is small enough, then neither diode will conduct strongly, and the effective resistance is very large (> 10 GΩ).

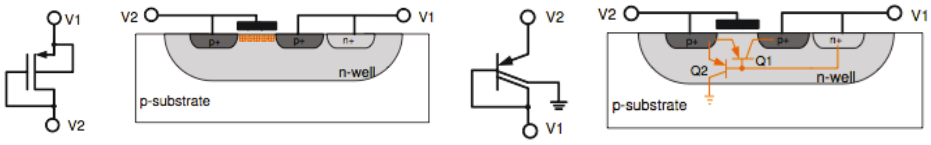

Fig. 1.13 Diode-connected and PN junction is forward-biased MOS transistor cross-section image

In that case when the voltage on V_1 larger then V_2 the MOS acts as the source of the transistor. For the opposite polarity, the driven side is a forward-biased source-gate junction.

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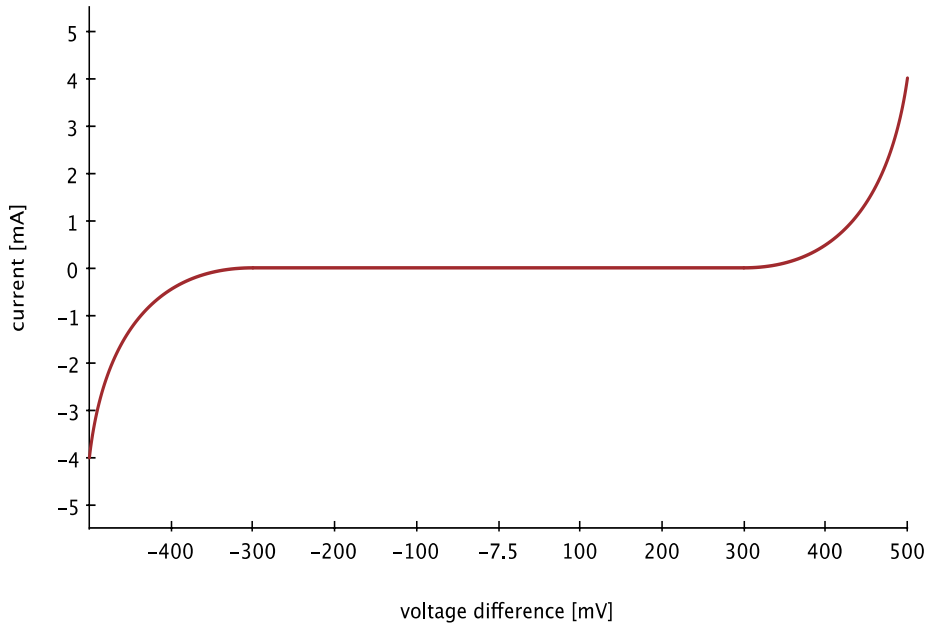

Fig 1.14 Current voltage relation on a pseudo-resistor

The current-voltage relationship (*Fig. 1.14*) [13, 20] of the expansive element means that the effective resistance of the element is large for small signals and small for large signals. Therefore, the adaptation is slow for small signals and fast for large signals.

The nonlinear variation of the resistance in the feedback loop means the transfer-function would not be permanent at the whole working period. If the cut of frequency is altered the whole distortion increases. This effect impairs significant in the lower frequency range (under 100 Hz). In my thesis I give a possible solution for this problem.

Another relevant problem to address with this solution is the large impact of the technological parameters and the operational conditions. The biomedical applications have strict operating requirement about the temperature (36.3-37 C°) that actually reduce the variation, but still remain large manufactured uncertainty (which depends on technology node).

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II. BASIC NEURO-AMPLIFIER TOPOLOGY

2.1 Feed-forward architecture

A feedforward amplifier topology instead of a feedback topology appeared to be a strong candidate for realizing low-power low-noise neural amplifier at first. I investigated the idea of using a feedforward distributed-gain amplifier topology to realize a low-power low-noise neural amplifier. Unfortunately, the topology posed some challenges that remained unsolved. However, the design insights obtained from the feedforward distributed-gain amplifier design led to a successful design of an energy-efficient neural amplifier which will be discussed later. In this chapter, I will present the basic ideas behind the feedforward distributed-gain amplifier and technical problems that I encountered during the design and verification phases that prevented this feedforward distributed gain amplifier to be used in real neural recording situations. To achieve the desired overall gain, the gain of the amplifier can be distributed among many stages. If the gain of the first stage is high, the total input-referred noise of the overall amplifier is dominated by the input-referred noise of the first stage. This idea can be illustrated with a two-stage amplifier shown in figure 2.1. The gain and the input-referred noise per unit bandwidth of the i^{th} stage are modeled as A_i and v_{ni}^2 respectively. The overall gain of the amplifier is $A = A_1A_2$.

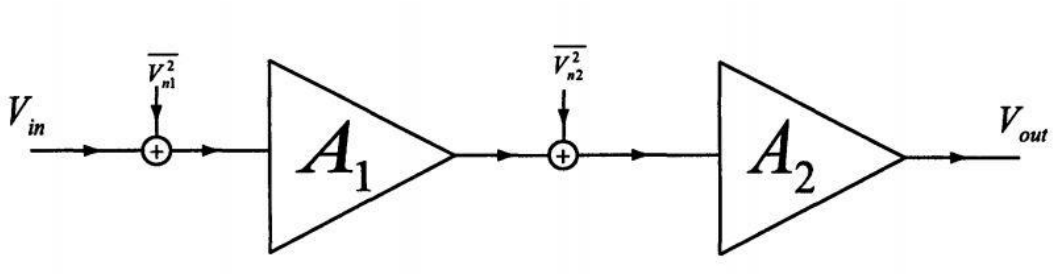

Figure 2.1 Schematic of a two-stage amplifier with input-referred noise sources

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We can then calculate the input-referred noise per unit bandwidth of the overall amplifier to be

$$v_{ni,in}^2 = v_{n1}^2 + \frac{v_{n2}^2}{A_1^2} \tag{2.1}$$

From (2.1) the input-referred noise power of the second-stage amplifier is attenuated by a factor of A_1^2. Therefore, if the first-stage amplifier's gain A_1 is high, the input referred noise requirement of the second-stage amplifier can be significantly relaxed. To achieve low-noise performance and desired overall gain, the first-stage amplifier should be designed to have low input-referred noise with enough gain while the subsequent stages just need to provide sufficient gains to meet the gain requirement for the overall amplifier while their input-referred noise requirements need not be as low as that of the first-stage amplifier. As discussed previously the input-referred thermal noise of the amplifier is proportional to $1/v_n^2$ where v_n, is the total input-referred noise of the amplifier. Therefore, subsequent amplifier stages' power consumptions can be significantly lowered without severely degrading their input-referred noise per unit bandwidth. Thus, for a distributed-gain amplifier, most of the overall power consumption should be consumed in the first-stage amplifier since its input-referred noise is the most critical and its gain should be sufficiently high such that the noise contributions from subsequent amplifier stages become insignificant.

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2.2 Feed-back architecture

Using the linear-region MOS transistors to set the DC operating points of the feed-forward distributed-gain amplifier poses a severe problem since the thermal noise in the linear-region MOS transistors appears at the frontend, which is the most critical stage of any low-noise amplifier. Instead of achieving a low-noise performance, the feed-forward distributed-gain amplifier have a much higher total integrated input-referred noise than it was originally desired due to these biasing elements. By setting the gate-source voltages of the linear-region MOS transistors such that the high-pass cutoff frequency of the amplifier happens at a very low frequency, the thermal noise in these linear-region MOS transistors can be filtered out well before the frequency band of interest. However, the robustness of the amplifier is compromised due to a very slow time constant caused by the high incremental resistance of these biasing elements. If there is any large fluctuation at the input of the amplifier during recording such as the movements of the electrode that cause the DC offset voltage at the electrode-tissue interface to change abruptly, the amplifier may stop amplifying for a period of several minutes before it resumes normal operation. This behavior is intolerable for a recording system, which needs to operate continuously once it is turned on. Therefore, a new amplifier that exhibits a lower input-referred noise and is also robust to changes in the recording environment is needed.

The folded-cascode OTA offers many advantages over other OTA topologies for low-frequency applications if it is used in a feedback topology with a high closed-loop gain. The first advantage is that the frequency compensation of the feedback amplifier can be achieved with simple dominant-pole compensation at the output since the internal nodes of the OTA have low impedances. Thus the non-dominant poles always appear at much higher frequencies than the dominant pole. Furthermore, the output impedance of the folded-cascode OTA is very high due to cascoding of the output stage, thus only one gain stage is needed to achieve a desired open-loop gain. The most important advantage is that for low-frequency applications such as in neural recordings, the current in the folded branch of the OTA can be made much lower than the current in the input differential-pair transistors without affecting the stability of the overall feedback amplifier. Lowering the current in the folded branch has two main benefits. First, the total power consumption of the OTA decreases. Second, the noise contributions from the transistors in the folded branch decrease due to a lower current level if the overall transconductance

of the OTA can be maintained. The design presented in this chapter makes use of this technique to try to simultaneously reduce the power consumption and the input-referred noise of the amplifier.

2.3 Amplifier Design

The high-level schematic of the amplifier is shown in figure 2.2. The MOS pseudoresistor elements M_{b1} and M_{b2} are used to set the DC operating point of the amplifier.

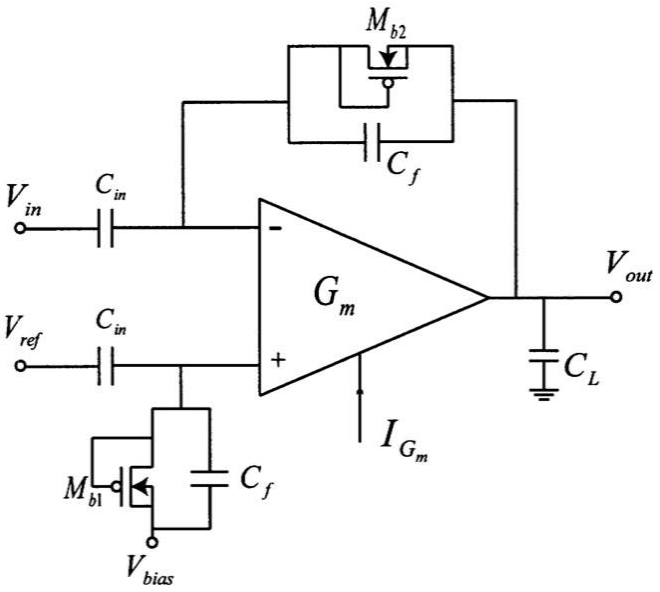

Figure 2.2: A high-level schematic of the feedback neural amplifier.

To understand why this feedback topology does not suffer from the robustness problem, let's consider the situation when there is a large fluctuation in the DC offset voltage at the recording site. Suppose that ΔV_{ref} experiences a voltage excursion of A_{Vref}. At the moment the voltage excursion occurs, the positive terminal's voltage of the G_m OTA will be at $V_+ = V_{bias}+C_{in}/(C_{in}+C_f) - \Delta V_{ref}$. If the feedback path formed by M_{b2} and C_f is not present and ΔV_{ref} is larger than the input linear range of G_m OTA, one of the transistors in the input differential pair of G_m OTA will carry all the bias current, making the amplifier to lose all its gain. Now let's consider when the feedback path is present. At the moment the input voltage excursion occurs, the G_m OTA has a large differential input voltage. Therefore, the output of the G_m OTA quickly moves toward and stays at one of the supply rails since the OTA has a very high gain. As a result, M_{b2} will have a large gate-source voltage. During this phase, M_{b2} no longer acts as a high-resistance element but becomes either a diode-connected MOS transistor or a diode-connected BJT

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depending on the output voltage polarities. The turned-on M_{b2} then quickly charges the voltage at the negative terminal V_- of the G_m OTA such that it becomes close to V_+ once again. As a result, the feedback topology can adjust to the fluctuations at the recording site much faster than the feed forward amplifier that uses the MOS-bipolar pseudoresistor elements to set the DC operating points. It was verified during the experiments that a large step change in DC input voltage does not cause the feedback amplifier to stop amplifying. Thus, this feedback amplifier is suitable for use in a real recording situation due to its robustness to the recording site's fluctuations.

Initial specification:

- supply voltage: 1.2 V
- Midband gain 50 dB
- Bandwidth: 0.1 Hz – 10 kHz
- Input signal parameter:
    - Amplitude: 50 µV – 1 mV
    - Offset: 500 mV
- Noise: 2 μV_{RMS}
- Area and power consumption as small as possible

2.4 Small-Signal Analysis

Let's analyze the operation of the amplifier in the Laplace's domain with the feedback block diagram approach. First, let us consider the operation of the gain stage. Let assume that the transfer function of the G_m OTA can be approximated by

$$A(s) = \frac{G_{m,eff}R_o}{(1+sR_oC_{L,p})} \tag{2.2}$$

where $G_{m,eff}$ and R_o are the effective total transconductance and the output resistance of the G_m OTA respectively. The loading effect at the output node of the gain stage is modeled as a $C_{L,p}$ parasitic capacitance and connecting between the output node of the gain stage to an incremental ground. Let $C_{in,p}$ denotes the parasitic capacitance connecting between the negative terminal of the G_m OTA to an

incremental ground. Let v_- denote the small-signal voltage at the negative terminal of G, OTA. Furthermore, let r_a denote the incremental resistance of M_{b2} when its gate-source voltage is close to zero. The circuit diagram for analyzing the operation of the gain stage is shown in figure 2.3. We can write v_- as a superposition of v_{in} and $v_{o,1}$ as

$$v_- = \frac{\frac{1}{sC_{in,p}} \left\| \frac{r_a}{1+sr_aC_f} \right.}{\frac{1}{sC_{in}} + \left(\frac{1}{sC_{in,p}} \left\| \frac{r_a}{1+sr_aC_f} \right. \right)} v_{in} + \frac{\frac{1}{s(C_{in,p}+C_{in})}}{\frac{1}{s(C_{in,p}+C_{in})} + \frac{r_a}{1+sr_aC_f}} v_{o,1} \tag{2.3}$$

$$= \frac{sr_aC_{in}}{1+sr_a(C_f+C_f+C_{in,p})} v_{in} + \frac{1+sr_aC_f}{1+sr_a(C_f+C_f+C_{in,p})} v_{o,1} \tag{2.4}$$

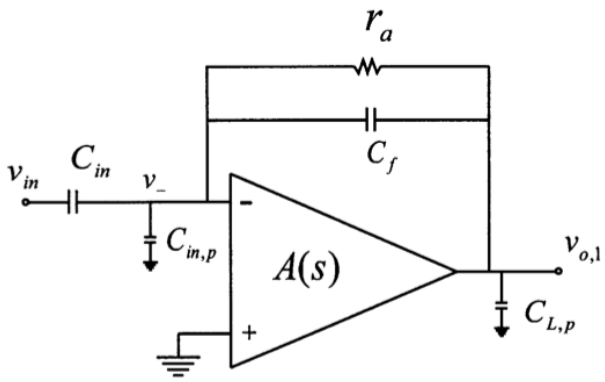

Figure 2.3: A circuit schematic for analyzing the operation of the folded-cascode gain stage.

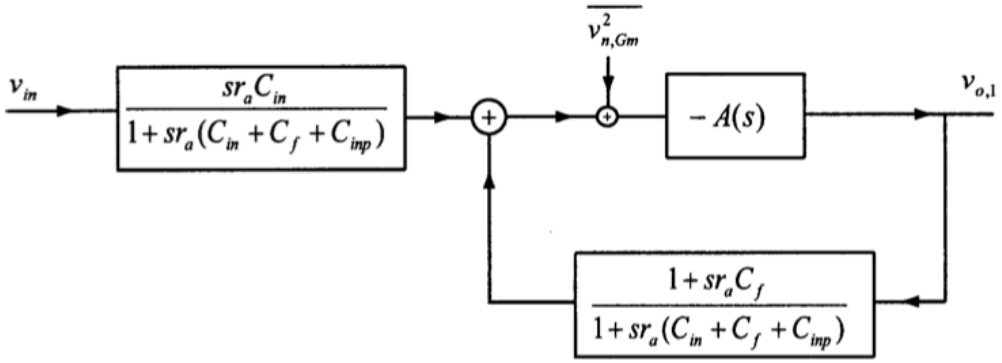

Figure 2.4: A preliminary block-diagram describing the operation of the feedback amplifier.

We can also write $v_{o,1}$ as a function of v_- as

$$v_{o,1} = -A(s)v_- \tag{2.5}$$

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Equations (2.3)-(2.5) can be captured in a feedback block diagram shown in figure 2.4. The input-referred noise of the G_m OTA is included in the block diagram with the $v_{n,Gm}^2$ term being added to the input of the G_m OTA, where $v_{n,Gm}^2$ represents the input-referred noise per unit bandwidth of the G_m OTA. The block diagram in Fig. 2.4 can be simplified into a unity-gain feedback form as shown in figure 2.5. In practice, the pole denoted by $1/(r_aC_f)$ is at a very low frequency (on the order of a few mHz). We can thus consider the operation of the amplifier when the frequency of operation $\omega \gg \frac{1}{r_{in}(C_{in}+C_f+C_{in,p})}$.

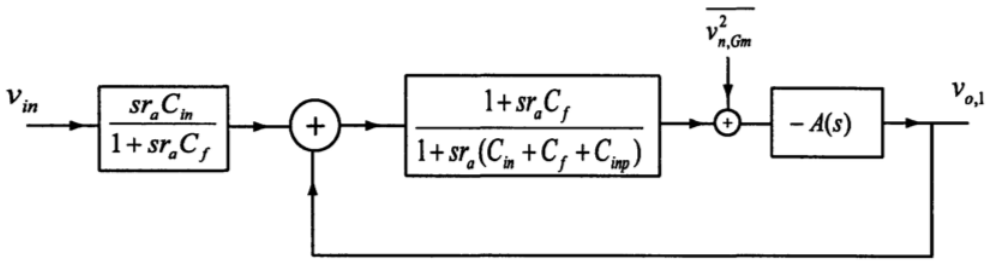

Figure 2.5: A unity-gain feedback block diagram describing the operation of the feedback amplifier.

Then the term $\frac{1+sr_aC_f}{1+sr_a(C_f+C_f+C_{in,p})}$ can be approximated by $\frac{C_f}{(C_{in}+C_f+C_{in,p})}$. Using (2.3) we can estimate the transfer function of the gain stage to be

$$\frac{v_{o,1}}{v_{in}}(s) \approx -\frac{sr_aC_{in}}{1+sr_aC_f}\frac{1}{1+sC_{L,p}\,A_{CL}/G_{m,eff}} \tag{2.6}$$

where $A_{CL} = \frac{(C_{in}+C_f+C_{in,p})}{C_f} \approx \frac{C_{in}}{C_f}$ is the closed-loop gain of the amplifier, assuming that $C_{in} >> C_f$, C_{inp}. Equation (2.2) suggests that the high pass cutoff frequency due to AC coupling is at $f_H = \frac{1}{r_aC_f}$ and the low pass cutoff frequency due to the loading effect at the output of the G_m OTA is at $f_L = \frac{G_{m,eff}}{2\pi A_{CL}C_{L,p}}$. Without an additional bandwidth-limiting stage we can't vary the bias current of the gain stage without affecting the overall bandwidth. At a midband frequency in which $\frac{1}{r_aC_f} < \omega < \frac{g_m}{C_L}$, the gain of the amplifier can be approximated by

$$A_M = -\frac{C_{in}}{C_f} \tag{2.7}$$

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As a result, the mid-band gain of the amplifier is controlled by the ratio of two capacitors and can be well controlled.

2.5 Noise Analysis

The amplifier can be thought of as a cascade of two amplifiers. The gain stage provides a midband gain of approximately 40 dB. From the feedback block diagram of figure 2.5, we can estimate the input-referred noise of the overall amplifier as

$$v_{n,amp}^2 = \left(\frac{C_{in}+C_f+C_{in,p}}{C_{in}}\right)^2 v_{n,G_m}^2 \tag{2.8}$$

Equation (2.5) emphasizes the importance of the parasitic capacitance C_{in}, at the negative input terminal of the OTA. While making the input differential-pair transistors large may reduce 1/f noise in the amplifier, the parasitic capacitances of large input devices can degrade the input-referred noise of the overall amplifier according to (2.8).

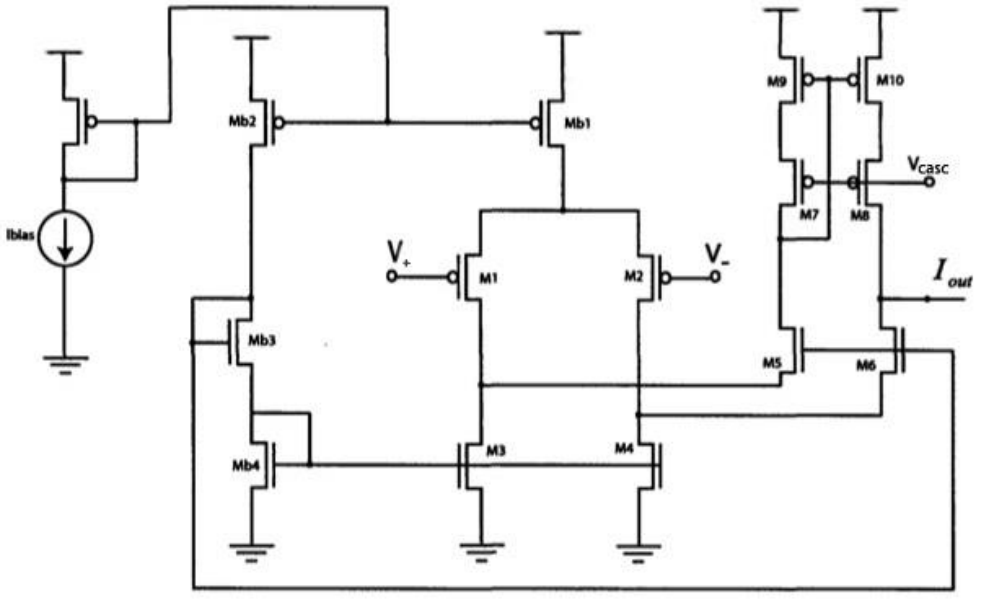

Figure 2.6: A folded cascade OTA schematic used in this design

To achieve a low-noise performance, the input-referred noise $v_n^2 G_m$ of the gain stage OTA must be minimized. This section discusses the low-noise techniques that figure 2.6: A folded-cascode OTA schematic used in this design are used in this design and also the implementation problems that prevent

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this design from achieving an optimal performance. The schematic of the folded-cascode OTA used in the gain stage. The OTA itself can be thought of as a two-stage amplifier. The first stage is the transconductance stage that has a voltage input and a current output. The second stage is a common-gate amplifier stage that takes in an input current and converts this current into a voltage at the output. The transconductance stage composes of M_{bl} and M_1-M_4 while the common-gate amplifier stage composes of M_5-M_{10}. We can express the folded-cascode OTA by their equivalent small-signal diagram as shown in figure 2.7. R_{ol} and R_{o2} are the output resistance of the transconductance stage and output resistance of the common-gate amplifier stage respectively and they can be approximated by

$$R_{o1} = r_{o2} \| r_{o4} \tag{2.9}$$

$$R_{o2} \approx ((g_{s8} r_{o8}) r_{o10}) \| ((g_{s6} r_{o6})(r_{o2} \| r_{o4})) \tag{2.10}$$

where r_{oi} and g_{si} are the output resistances and the incremental source admittance of M_i respectively.

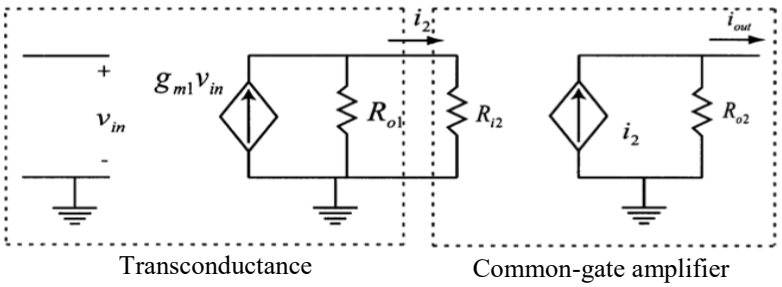

Figure 2.7: A small-signal schematic for describing the operation of folded-cascode OTA.

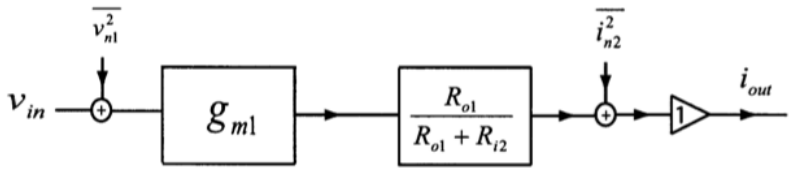

Figure 2.8: A small-signal block diagram describing the operation of folded-cascode OTA.

The resistance R_{i2} is the input resistance of the common-gate amplifier stage, which can be approximated by

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$$R_{i2} = \frac{1}{g_{s5}} \tag{2.11}$$

where g_{s5} is the incremental source admittance of M_5 and M_6.

The noise analysis of the OTA can be best understood by the small-signal block diagram shown in figure 2.7. The amount of the transconductance stage's output current that flows into the source of M_5 and M_6 is determined by the current divider formed by R_{o1} and R_{i2}. The current that flows into R_{i2} appears directly at the output of the common-gate stage. This is described by a unity-gain buffer. The input-referred noise of the transconductance stage is represented by $v_n^2{}_1$ while the input-referred noise of the common-gate stage which has a current input is represented with a current noise source $i_n^2{}_{,2}$.

The input-referred noise of the transconductance stage can be calculated to be

$$v_{n,1}^2 = \frac{1}{g_{m1}^2}\left(i_{n,M1}^2 + i_{n,M2}^2 + i_{n,M3}^2 + i_{n,M4}^2\right) \tag{2.12}$$

In order to minimize this input-referred noise, we shall maximize g_{m1}. Therefore, the input differential-pair transistors M_1 and M_2 are made with large W/L such that they operate in deep in subthreshold and achieve the maximum g_m for a given bias current. Even though M_3 and M_4 should be biased in strong inversion to reduce their g_m in order to reduce their noise contribution, in this design they operate in subthreshold so that their saturation voltages can be small. The amplifier was designed to work with a 2V supply, thus minimizing the noise contributions from M_3 and M_4 by operating them well above threshold proved to be impractical. Thus, the input-referred noise of the transconductance stage can be expressed in terms of the transistors' small-signal parameters as

$$v_{n,1}^2 = \frac{2kT}{\kappa g_{m1}}\left(2 + 2\frac{g_{m3}}{g_{m1}}\right) \tag{2.13}$$

To simplify the input-referred noise calculation of the common-gate amplifier stage, we make an assumption that the noise contributions from M_5-M_6 are negligible since they act as cascode transistors and these transistors self-shunt their own current noise sources. Thus the transistors in the common-gate amplifier stage that significantly contribute noises are M_9 and M_{10}. Due to supply voltage constraint, M_9 and M_{10} are also biased in weak-inversion such that they can operate with small saturation voltages. Thus, the input-referred current noise of the common-gate amplifier stage can be expressed as

$$i_{n2}^2 = i_{n,M9}^2 + i_{n,M10}^2 \tag{2.14}$$

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$$= 2\frac{2kT}{\kappa} g_{m9} \tag{2.15}$$

Let $G_{m,eff}$ be an effective total transconductance of the folded-cascode OTA. From the circuit diagram in figure 2.6. It can be calculated

$$G_{m,eff} = \frac{i_{out}}{v_{in}} = g_{m1}\frac{R_{o1}}{R_{o1}+R_{i2}} \tag{2.16}$$

Thus the total input-referred voltage noise of the OTA can be expressed as

$$v_{n,OTA}^2 = v_{n1}^2 + \frac{1}{G_{m,eff}^2} i_{n2}^2 \tag{2.17}$$

$$= \frac{4kT}{\kappa g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}} + \left(\frac{R_{o1}+R_{i2}}{R_{o1}}\right)^2 \left(\frac{g_{m9}}{g_{m1}}\right)\right) \tag{2.18}$$

In order to minimize the input-referred noise for a given bias current, g_{m9} should be maximized by operating M_1 and M_2 in subthreshold. Furthermore the g_{m9} and the current divider ratio $\frac{R_{o1}+R_{i2}}{R_{o1}}$ should be minimized. In this design, the current in M_9 and M_{10} to be much smaller than the current in M_1 and M_2. In this way, the ratio g_{m9}/g_{m1} is made small compared to other terms in (2.17). Moreover, lowering the current in the folded branch makes the term g_{m3}/g_{ml}, which is usually larger than 1 becomes close to 1 since the currents in M_3 and M_4 are almost the same as the current in M_1 and M_2. For this topology, the ideal input-referred noise that can be achieved while all the transistors are operating in subthreshold is

$$v_{n,OTA}^2 = 4\frac{2kT}{\kappa g_{m1}} \tag{2.19}$$

assuming that $g_{m3} \approx g_{m1}$ and $g_{m9}/g_{ml} << 1$. The ideal input-referred noise in (2.18) is equivalent to the input-referred noise of an OTA with effectively four subthreshold devices that contribute noise.

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2.6 Differential output Folded-Cascode OTA using as the Gain Stage

The folded-cascode OTA offers many advantages over other OTA topologies for low-frequency applications if it is used in a feedback topology with a high closed-loop gain. The first advantage is that the frequency compensation of the feedback amplifier can be achieved with simple dominant-pole compensation at the output since the internal nodes of the OTA have low impedances. Thus the non-dominant poles always appear at much higher frequencies than the dominant pole. Furthermore, the output impedance of the folded-cascode OTA is very high due to cascoding of the output stage, thus only one gain stage is needed to achieve a desired open-loop gain. The most important advantage is that for low-frequency applications such as in neural recordings, the current in the folded branch of the OTA can be made much lower than the current in the input differential-pair transistors without affecting the stability of the overall feedback amplifier. Lowering the current in the folded branch has two main benefits. First, the total power consumption of the OTA decreases. Second, the noise contributions from the transistors in the folded branch decrease due to a lower current level if the overall transconductance of the OTA can be maintained. The design presented in this chapter makes use of this technique to try to simultaneously reduce the power consumption and the input-referred noise of the amplifier. However, the fabricated amplifier exhibited poor performance since many design issues were overlooked.

The MOS-bipolar pseudo-resistor elements are used to set the DC operating point of the amplifier. To understand why this feedback topology does not suffer from the robustness problem, let's consider the situation when there is a large fluctuation in the DC offset voltage at the recording site. Suppose that V_{ref} experiences a voltage excursion of ΔV_{ref}. At the moment the voltage excursion occurs, the positive terminal's voltage of the g_m OTA will be at $V_+ = V_{bias}, + C_{in}/(C_{in}+C_f)+\Delta V_{ref}$. If the feedback path formed by the pseudo-resistor and C_f is not present and ΔV_{ref} is larger than the input linear range of g_m OTA, one of the transistors in the input differential pair of g_m OTA will carry all the bias current, making the amplifier to lose all its gain. Now let's consider when the feedback path is present. At the moment the input voltage excursion occurs, the g_m OTA has a large differential input voltage. Therefore, the output of the g_m OTA quickly moves toward and stays at one of the supply rails since the OTA has a very high gain. Than the pseudo-resistor will have a large gate-source voltage. During this phase, it is no longer

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acts as a high-resistance element, but becomes either a diode-connected MOS transistor or a diode-connected BJT depending on the output voltage polarities. The turned-on the resistor then quickly charges the voltage at the negative terminal V_- of the g_m OTA such that it becomes close to V_+ once again. As a result, the feedback topology can adjust to the fluctuations at the recording site much faster than the feed-forward amplifier that uses the MOS-bipolar pseudo-resistor elements to set the DC operating points. It was verified during the experiments that a large step change in DC input voltage does not cause the feedback amplifier to stop amplifying. Thus, this feedback amplifier is suitable for use in a real recording situation due to its robustness to the recording site's fluctuations.

Consequently, the amplifier is based around an operational transconductance amplifier that produces a current applied to its input (Fig. 2.9) [9,11,20-22]. A capacitive feedback network consisting of C_1 and C_2 capacitors sets the mid-band gain of the amplifier. The input is capacitively coupled through C_1, so any dc offset from the electrode-tissue interface is removed. C_1 should be made much smaller than the electrode impedance to minimize signal attenuation. The R_2 elements shown in the feedback loop set the low-frequency amplifier cut-off.

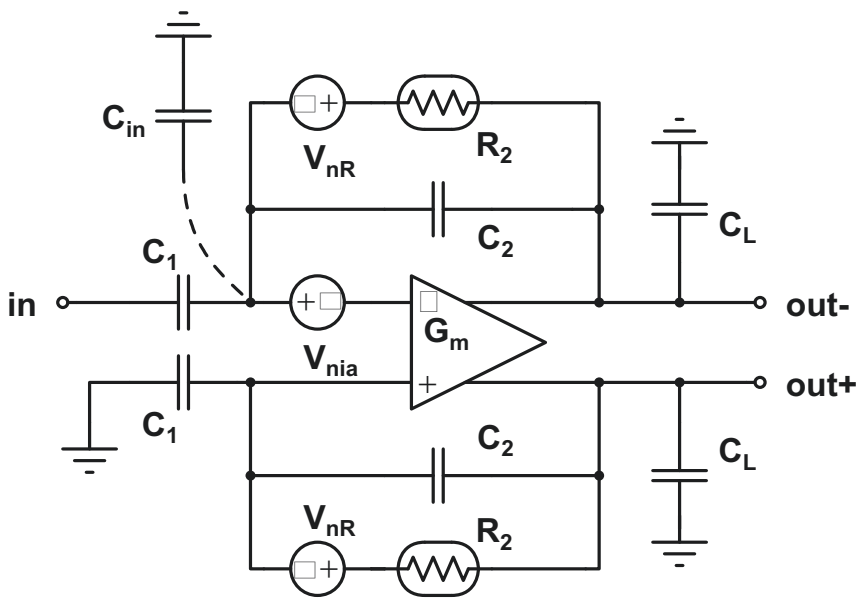

Figure 2.9 Schematic of the capacitive feedback amplifier

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The approximate transfer function is given by

$$\frac{v_{out+}-v_{out-}}{v_{in}} = \frac{C_1}{C_2}\frac{1-sC_2/G_m}{\left(\frac{1}{sR_2C_2+1}\right)\left(s\frac{C_LC_1}{G_mC_2}+1\right)} \tag{2.20}$$

The midband gain A_M is set by the capacitance ratio C_1/C_2, and the gain is flat between the lower and upper cutoff frequencies f_L and f_H. The product of R_2 and C_2 determines the lower cutoff frequency, while the upper cutoff is determined by the load capacitance C_L, the OTA trans-conductance g_m, and the mid-band gain. Capacitive feed introduces a right-half-plane zero at f_z, but this zero can be very at high frequency by setting

$$C_2 \ll \sqrt{C_1C_L} \tag{2.21}$$

so that it has little practical effect on amplifier operation. The OTA contributes noise primarily between f_L and f_H. Below a particular frequency called f_{corner}, the noise contribution from v_{nR} will dominate. If R_2 is implemented as a real resistor so that its noise spectral density is

$$v_{nR}^2(f) = 4kTR_2 \tag{2.22}$$

and $C_1 >> C_2$, C_{in}, then f_{corner} is approximately

$$f_{corner} \approx \sqrt{\frac{3C_L}{2C_1}f_Lf_H} \tag{2.23}$$

A similar result is obtained for pseudo resistor element used as R_2 in. To minimize the noise contribution from the R_2 elements, we should ensure that $f_{corner} << f_H$.

If the noise contribution from R_2 is negligible and $C_1 >> C_2$, C_{in}, then the output *rms* noise voltage of the neural amplifier is dominated by the noise from the OTA.

$$v_{nia}^2 = \frac{16kT}{3g_{m1}}\left(1+2\frac{g_{m3}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right) \tag{2.24}$$

where g_{m1} is the trans-conductance of the input devices M_1 and M_2. The noise of the cascode transistors is negligible.

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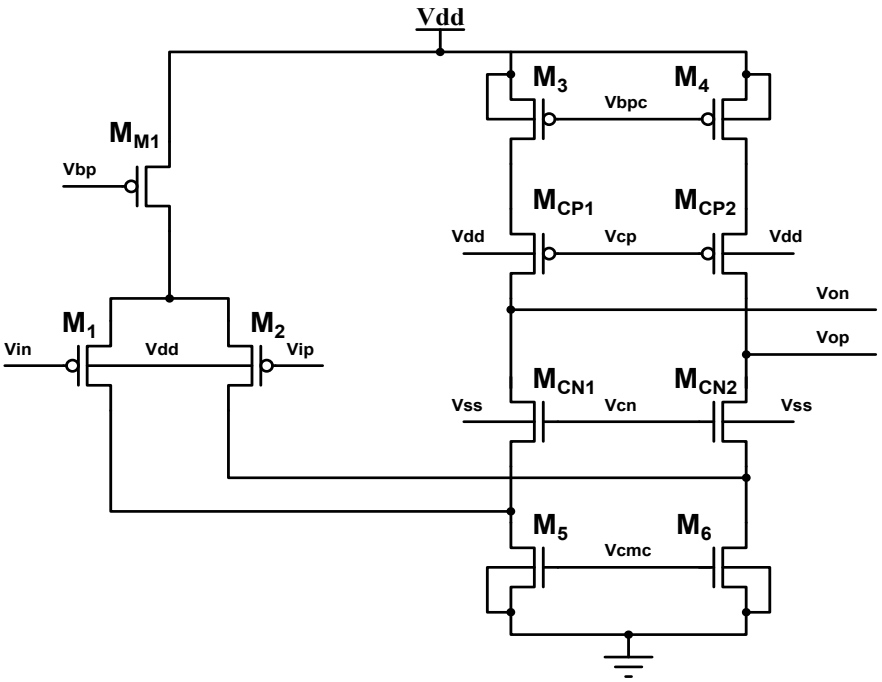

Fig. 2.10 Differential input cascoded OTA

In that case the load capacitance is determined by

$$C_L = \frac{4kT}{V_{ni}^2 3A_M} \tag{2.25}$$

Element	W/L size [μm]
M_{M1}	28/2.5
M_1/M_2	640/1
M_3/M_4	3.5/1
M_{CP1}/M_{CP2}	5/1
M_{CN1}/M_{CN2}	4/1
M_5/M_6	29/1

Table 2.1 Transistor size chart for the CMFB

In practical implantable multi electrode systems, the size of the capacitances is limited. On the one hand it is due to the minimal size of the C_2 with tolerable fabrication variance. On the other hand, the available space set the maximum for the C_1. The ratio between the capacitances defines the amplification magnitude.

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In order to cancel the common-mode current component in the differential output it is necessary to use a feedback circuit, which compares the common mode voltage with a reference and correct the common-mode level. The implementation of this circuit can be seen on figure 2.11, where V_{on} and V_{op} are the outputs of the OTA. The V_{bp} and V_{cn} are biasing the circuit and the V_{cm} is the desired common-mode level. The V_{cmc} is the feedback signal for the amplifier. In table 2.1 and 2.2 the used transistor dimensions can be seen respectively for the OTA and the common mode feedback (CMFB) circuit.

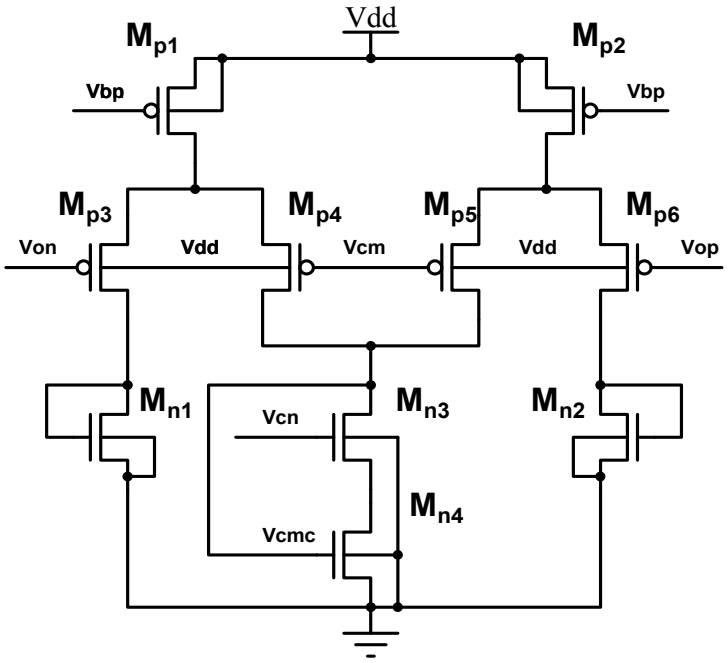

Figure 2.11 Common mode feedback for the amplifier

Element	W/L size [μm]
M_{p1}/M_{p2}	1/5
$M_{p3}/M_{p4}/M_{p5}/M_{p6}$	5/1
M_{n1}/M_{n2}	0.5/4
M_{n3}	2/1
M_{n4}	1/9

Table 2.2. Transistor size chart for the CMFB

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III. SERIES-CONNECTED DIGITALLY CONTROLLABLE PSEUDO-RESISTOR

There is a possible tradeoff between the noise and distortion. Using more pseudo resistor element in series helps decreasing the nonlinearity effect at the price of increasing noise figure. In this section this tradeoff is analyzed on resistor-chains, which contain different number of pseudo resistor element. Because no one examined that before it leads me to a discovery what I write down in a thesis (I).

The series of pseudo-resistors results in decreasing distortion approximately linearly with the number of elements, due to the voltage different would be smaller between the two sides of each element (Fig. 3.1).

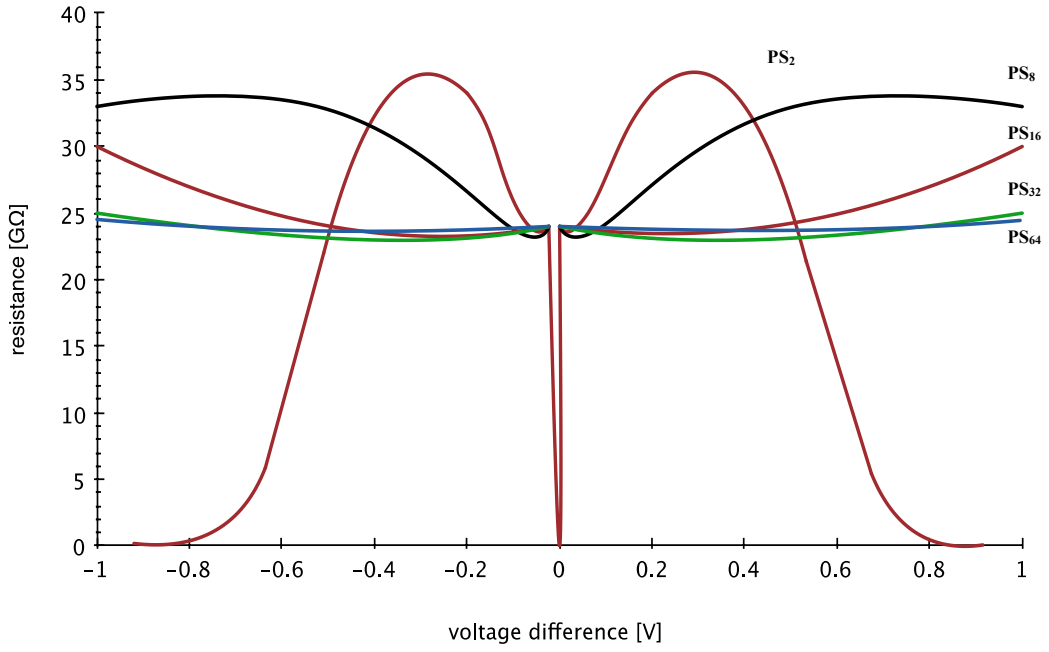

Figure 3.1 Resistance variation at different number pseudo-resistor in series

(curves PS2, PS8, PS16, PS32, PS64 respectively) [GΩ / V]

In order to fulfill the accuracy requirements in the whole system, we need satisfy the total harmonic distortion (THD) on every frequency as well. For a typical 8-bit accuracy case, we would need to keep at least the 60 dB level for the frequency range of interest (Fig. 3.2).

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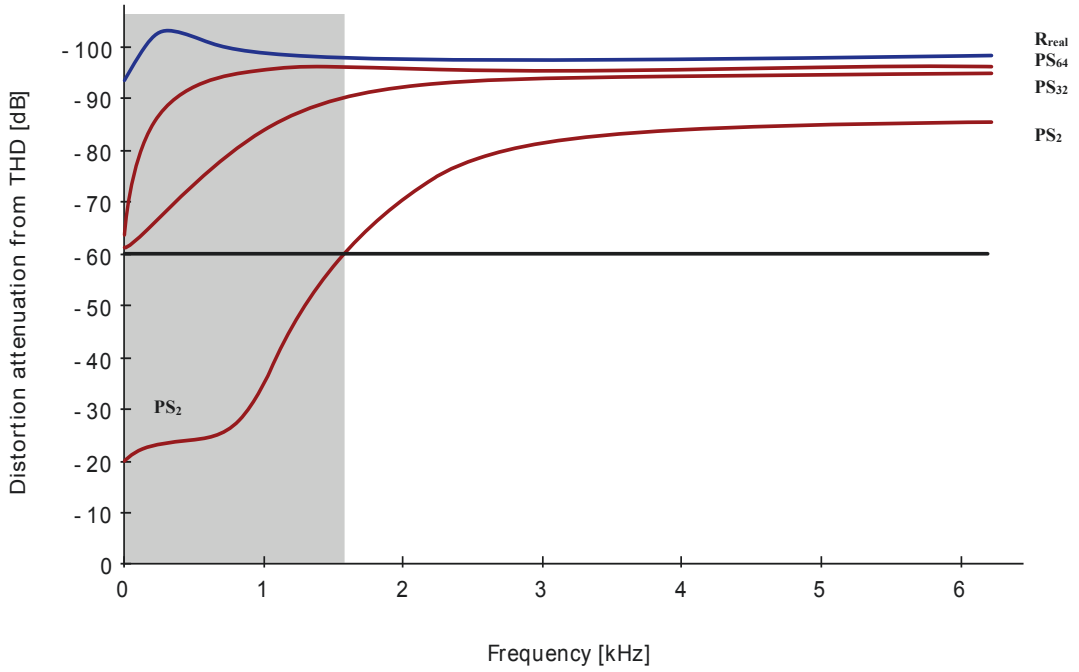

Figure 3.2 THD with different resistor implementation showing the constraint for a typical -60 dB system

Because of the high corner deviations and the frequency tune-ability, another important aspect in the design is the resistance control.

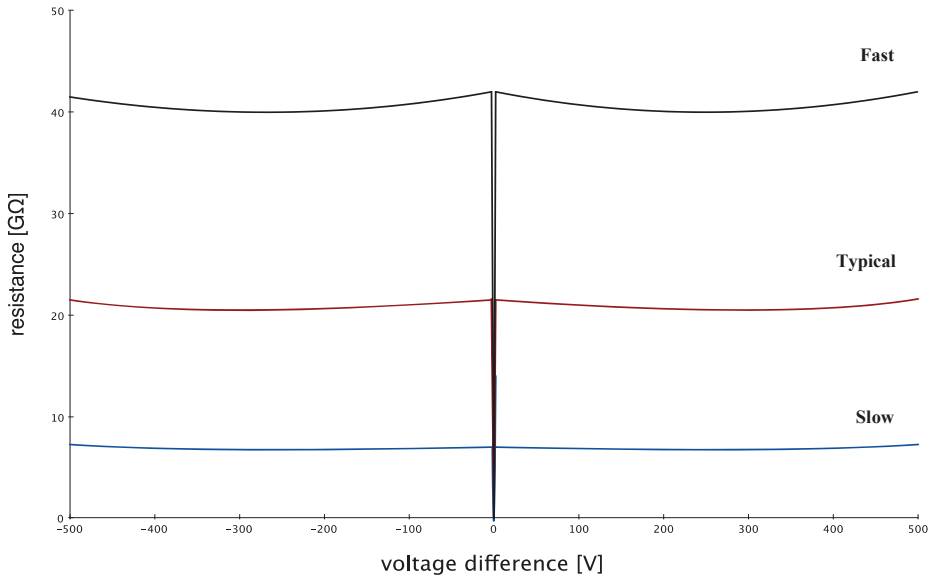

Figure 3.3 PS_{32} Resistance variation in different corners, caused by the temperature and supply voltage variation

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It possible to give controllability to the resistance if we use switches to shortcut the remaining part of the chain (Fig. 3.3). This gated structure needs to be designed at least the required resistance plus the corner variations. Note that the large number of the series connected pseudo resistor still does not have area large overhead neither the parasitic.

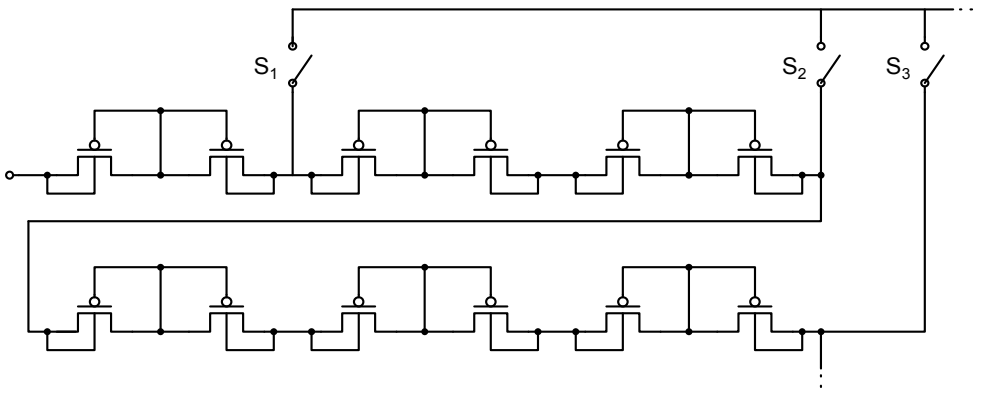

Figure 3.4 Gated pseudo-resistance chain

The switch implementation needs careful design as well. Large open state impedance is required so that they could be commensurable to the pseudo-resistances, otherwise the leakage will reduce the overall resistance; hence they must be optimized to the OFF resistance oppositely the general usage.

Another issue is how to scale the different segments in the resistor chain. It is not effective to use identical number of resistors in each segment if we want to tune and compensate with the same chain (Fig. 3.4), because the tuning and the compensation need different size of variation. The exact choice of distribution (linear, exponential, or binary weighted) depends on the required cut-off frequencies and the degree of the corner deviations.

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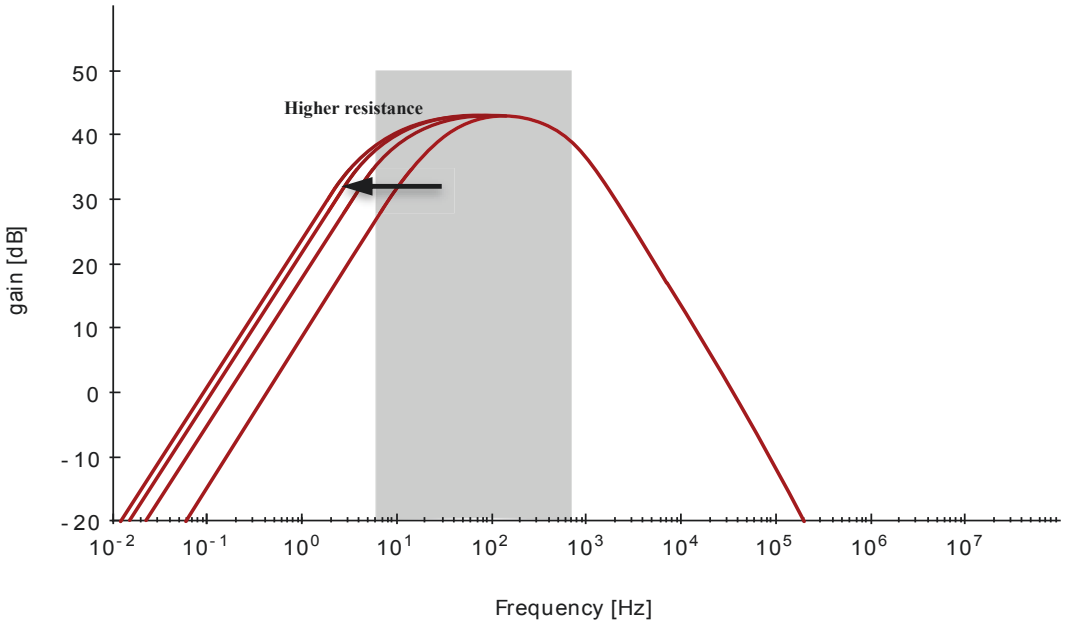

Figure 3.5.a Transfer function at different f_L

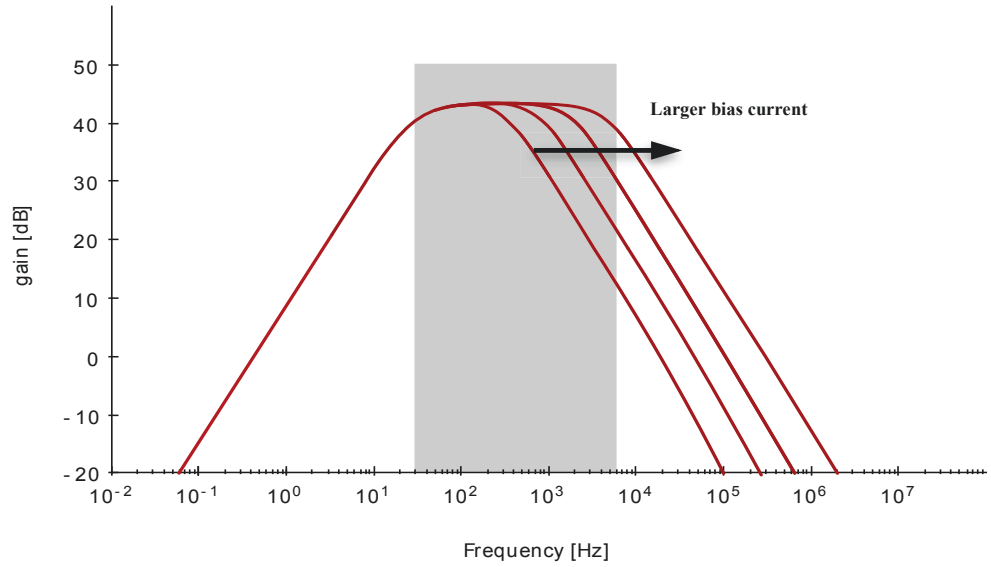

Figure 3.5.b Transfer function at different f_H

Finally, we got a programmable solution that helps us to increase the robustness against the technology parameter variation, to reduce the significant distortion and gives us the possibility to choose the cut-off frequency.

Using different bias current generate different noise in the amplifier (Table 3.1), therefore we need to choose carefully the optimal current.

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Current [A]	Noise [μV_{RMS}]
50n	6,8
100n	6,6
500n	6,1
1u	5,9

Table 3.1. Different bias current influence on noise
(simulated comparison)

Creating a design flow (Fig. 3.6) can help us to design another bio-amplifier with different technology or specification.

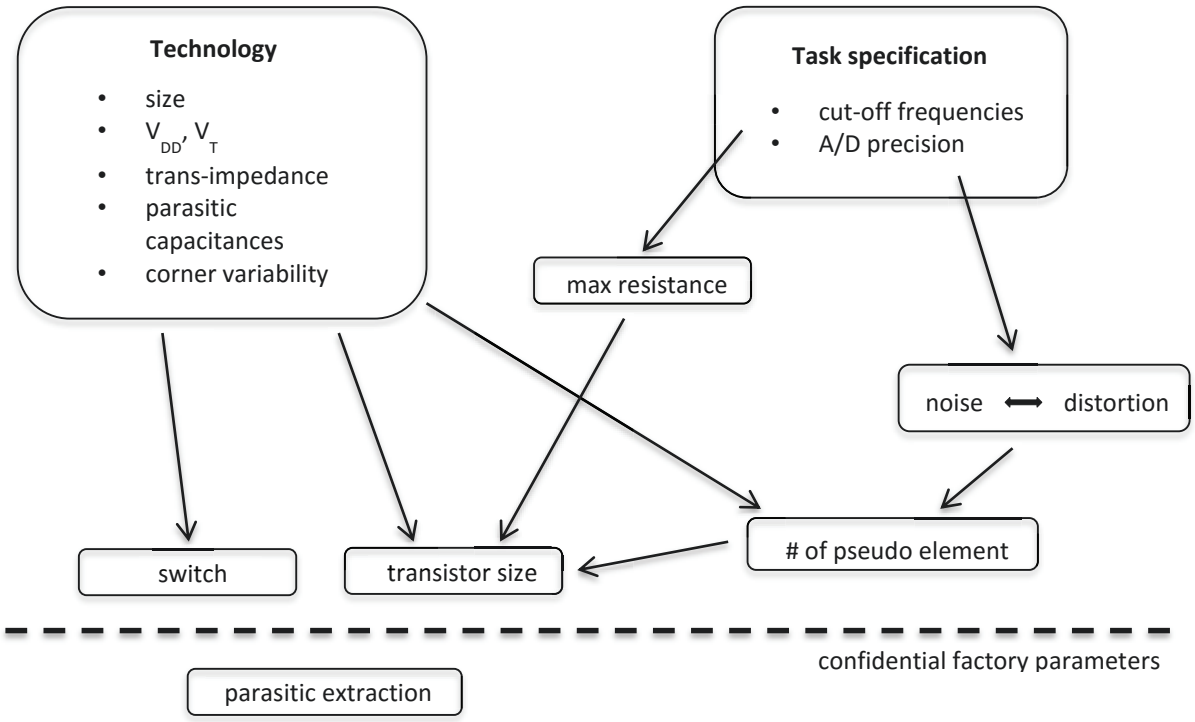

Figure 3.6 Design flow for the amplifier design

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To determine the resistance of each pseudo element it must be calculated analytically the resistance from the BSIM3v3 transistor model parameters.

$$\frac{V_{OUT}}{V_{IN}} = \frac{(G_{BS_1}+G_{DS_1})(G_{BD_2}+G_{DS_2})}{G_{BD_2}+G_{BS_1}+G_{DS_1}+G_{DS_2}+G_{BD_2}G_{BS_1}+G_{BD_2}G_{DS_1}+G_{BS_1}G_{DS_2}+G_{DS_1}G_{DS_2}} \tag{3.1}$$

Self-compensation

The next step was to find a quasi-automatic solution to get the required steady resistance value in normal operational condition. Even reduce resistance variations in different corner situations like the case of higher or lower temperature or supply voltage. The basic idea was to find a reference resistor with the same input and use a voltage difference with opposite sign to reduce or even extinguish the resistance variation effect.

The first solution is a double chain where the master line length can be shortening if the voltage is dropped, so the resistance can keep the same level. It was the necessary to add comparators for the proper switching and the higher default resistance to reduce the parallel connection.

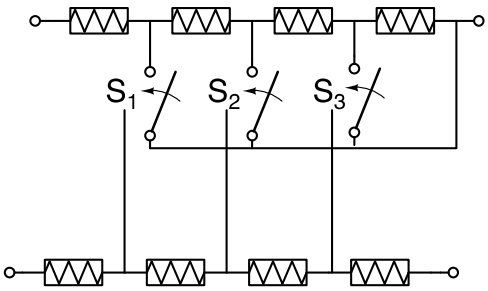

Figure 3.7 Segment of a symmetry based double chain

The second version based on current mirror, but operates the same way as the double chain. In the final design I had to implement many long transistors to reach the desired resistance to compensate the variation which lead to higher noise and current consumption.

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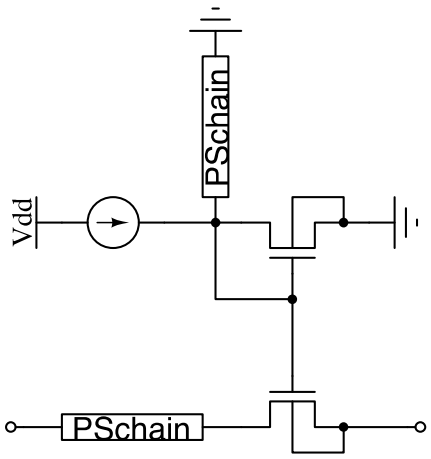

Figure 3.8 Current mirror controlled chain

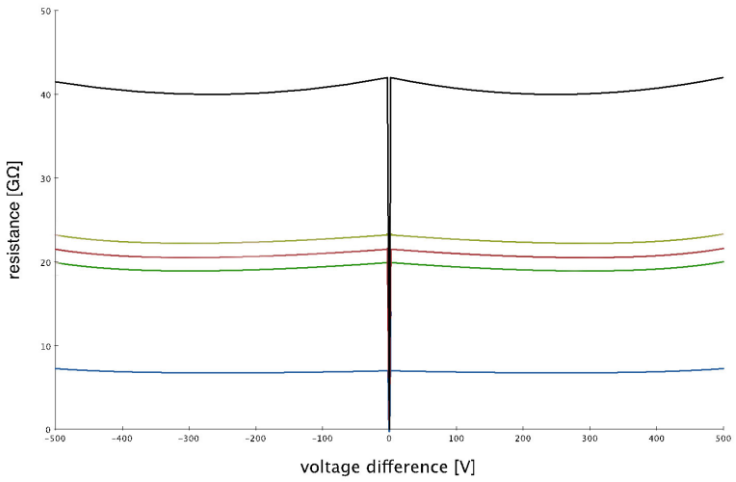

Figure 3.9 Comparison between the compensated double chain and the standard solution

Disadvantage of this solution is the higher space requirement, which at least twice of the size as the simple chain. Unfortunately, the size of the pseudo resistors is already a significant part of the layout. While the gain as the high-cutoff frequency can be define more precise can be neglected in our research condition. Specifically, it is not relevant if f_L is 30, 50 or 70 mHz. However, it is working concept which could be useful in other situation. Due to that drawbacks this version was not implemented.

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Distortion supplemented Noise Efficiency Factor

The noise-power tradeoff is characterized by the Noise Efficiency Factor (NEF).

$$NEF = v_{in,rms}\sqrt{\frac{2I_{tot}}{\pi V_t 4kT\, BW}} \tag{3.2}$$

where $v_{in,rms}$ is the total equivalent input noise, BW is the 3-dB bandwidth of the amplifier, refers to the thermal voltage, and I_{tot} is the average current consumption of each amplifier in the proposed architecture. The noise efficiency factor gives a good number to determine the connection between the noise and power consumption, but it doesn't say anything about the distortion. If we take the maximal THD factor over the amplification range and convert to percent value, then we can multiply the NEF with it. With -40dB distortion we got the same value as before.

The Distortion supplemented Noise Efficiency Factor (DNEF) is a NEF weighted by the average THD value. The calculation of this parameter can be seen on the 3.3 equation. The main advantages for using this parameter over the NEF that it gives more details about the LNA performance concerning the distortion value and helps to compare the power, noise and distortion parameters between different amplifier design. Table 3.2 shows the difference between the NEF and DNEF.

$$DNEF = NEF\ 20\ lg\frac{\max(THD)}{100} \tag{3.3}$$

Parameter	[5]	[28]	This work
-3 dB Bandwidth	7.2 kHz	0.3~10 kHz	2.8 Hz~8.1(10) kHz
Input Referred Noise [μV_{RMS}]	2.2	4.9	5.9 (6.2)
Noise Efficiency Factor	4	5.99	4.9
THD [%]	1@16 mV_{pp}	2@200 μV_{pp}	0.1@10 mV_{pp}
DNEF	4	11.98	0.49

Table 3.2 NEF and DNEF comparison

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IV. MEASUREMENTS AND CONCLUSION

In order to prove the theory and verify simulations we designed the architecture with 32 pseudo-resistors chain and a low power LNA. The targeted technology was the TSMC 90 nm LP-RF [29]. The fabricated chip layout can be seen on figure 4.1, a second developed version on figure 4.2 and micro-photo of the two amplifiers on figure 4.3.

The first test was performed to deal with electrical parameters, then we made the experiments with the multi-probe electrode [18] on rodents. The measured parameters are shown in Table 4.1 and 4.2. The different bias current implies different noise and power consumption.

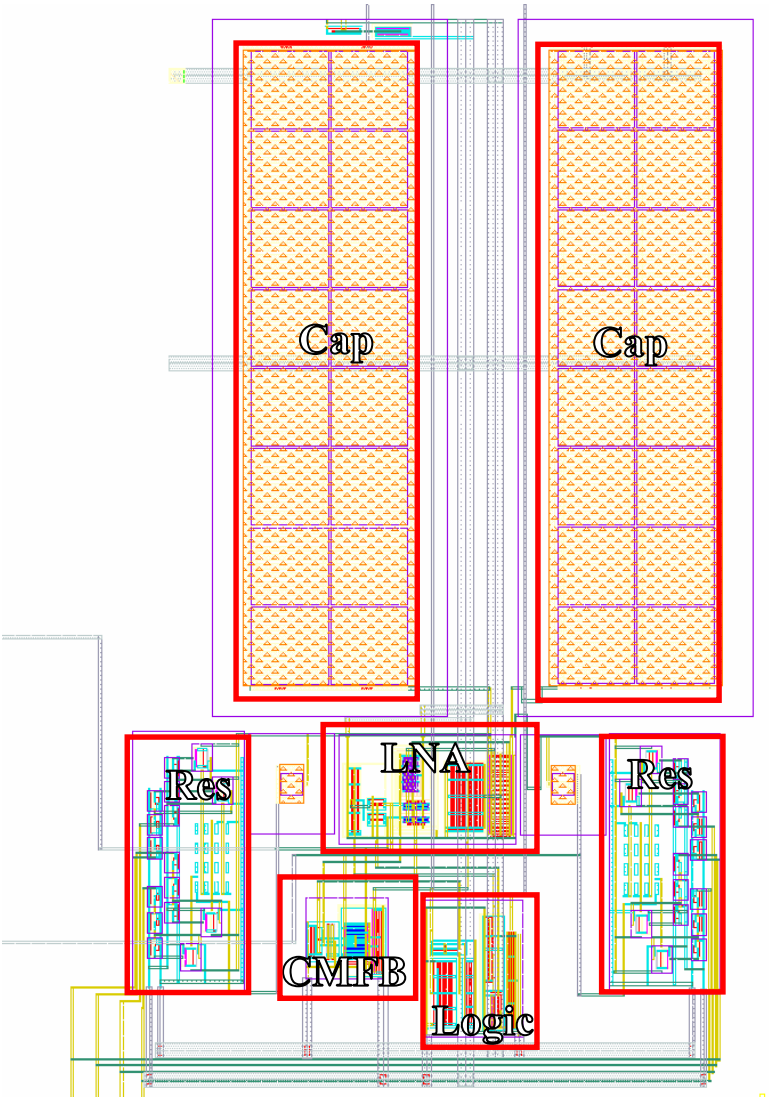

Figure 4.1 Layout of the revision A chip

DOI:10.15774/PPKE.ITK.2016.005

Parameter	[5]	[21]	[22]	[27]	[28]	This work
Supply Voltage [V]	2.5	3	3	1.2	0.5	1.2
Process Technology	0.5 µm	350nm	350nm	130nm	65nm	90 nm
Midband Gain [dB]	39.5	37.5	6-47	40	40-56	44.1 (44)
-3 dB Bandwidth	7.2 kHz	1~10 kHz	0.1-12 kHz	10 kHz	0.3~10 kHz	2.8 Hz~8.1(10) kHz
Input Referred Noise [μV_{RMS}]	2.2	10.6	2.95	2.2	4.9	5.9 (6.2)
Noise Efficiency Factor	4	5.78	3.1	6.25	5.99	4.9
THD [%]	1@16 mV_{pp}	-	-	-	2@200 μV_{pp}	0.1@10 mV_{pp}
CMRR [dB]	83	74	99	-	75	73 (78)
PSRR [dB]	85	55	85	-	64	81 (90)
Tunable cut-off frequency	-	-	+	+	+	+
Variable gain	-	-	+	-	+/-	-
Power [µW]/ch.	16	6	27	68	15	0.7 - 4.6
Area [mm^2]/ch.	0.16	0.058	0.08	0.013	0.25	0.025

Table 4.1 Amplifier performance comparison based on the electrical measurements.
The simulation results can be found in parenthesis.

Current [A]	Noise [μV_{RMS}]
50n	4,8
100n	4,6
500n	4,1
1u	3,9

Table 4.2 Different bias current influence on noise

The amount of parasitic is partly determined by the transistor geometry that can therefore be optimized for a given application. Usually for analog applications, wide transistors are used (several microns width). Instead of using one wide gate, the transistor is folded to decrease the total active area (and thereby the junction capacitance) and the gate resistance. The gate resistance is further reduced when connected at both sides. Finally, the bulk resistance is minimized when a guard ring is designed. These layout tricks are key for analog applications since f_{max} depends greatly on both gate and substrate resistances. Furthermore, a square layout is favorable to reduce process-induced variations within a device and therefore the matching. Reducing the offset can be achieved with transistors, small effective gate-source voltages of the input transistors and small W/L ratio of the current mirror and the current. Thermal noise can be reduced by using large g_m of the input transistors and small W/L ratio of the current mirror and the bias sources. While the flicker noise (1/f) can be lower using large area of the input transistors and increase the length of the current mirror and the current sources which reduce the unit difference between the branches.

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The chip layout can be seen on figure 4.2 and a micro-photo on figure 4.3. The most striking change in the second version of this chip is the larger capacitance which are placed over the transistors to save space on the layout. A differential and a single ended version was designed in order to compare the difference in parameters.

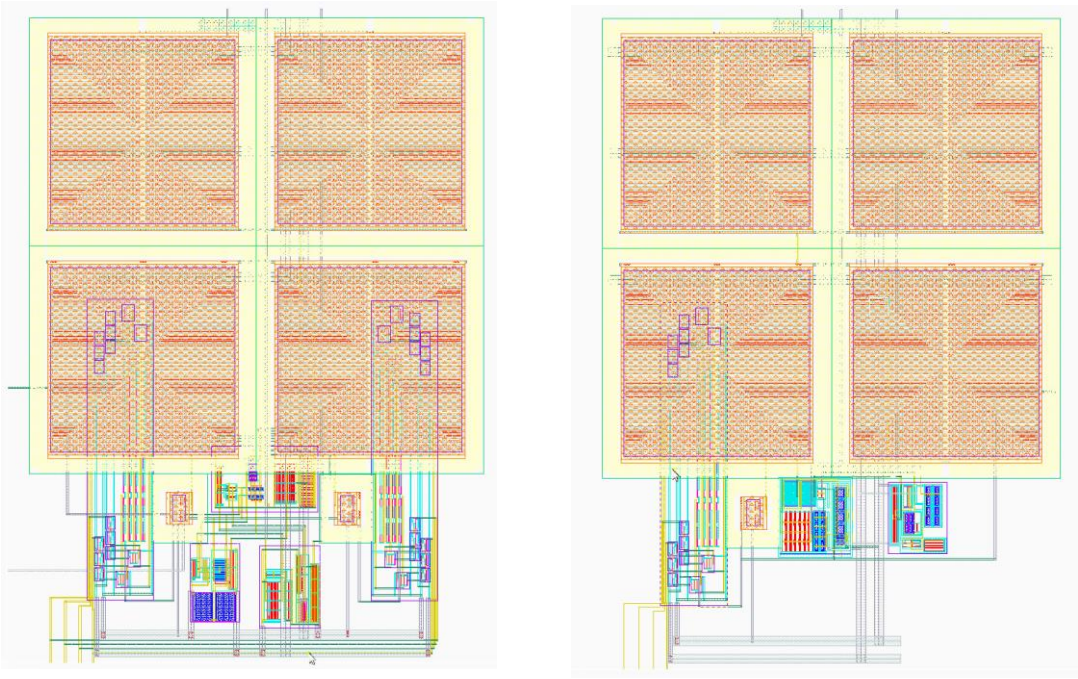

Figure 4.2. Layout of the differential and single ended solution

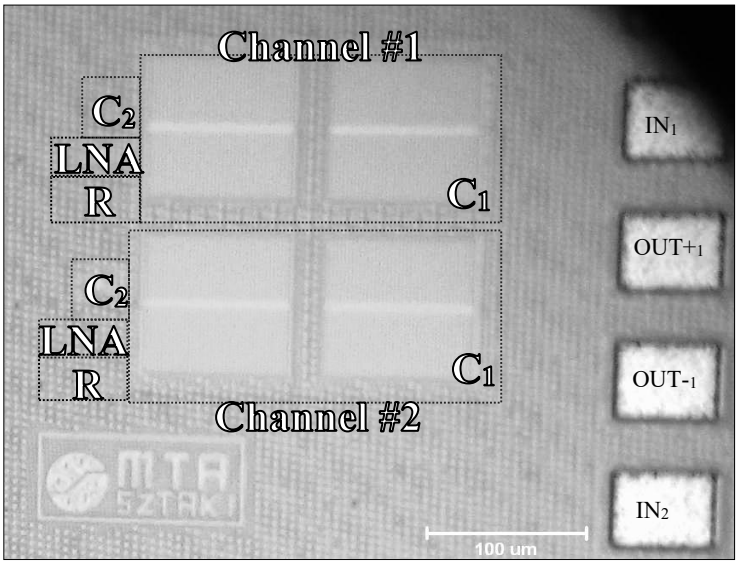

Figure 4.3 Micro photo of two-channel interface

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Like every analog layout here also used the interleaving technique to reduce the offset between the differential pair and current mirrors.

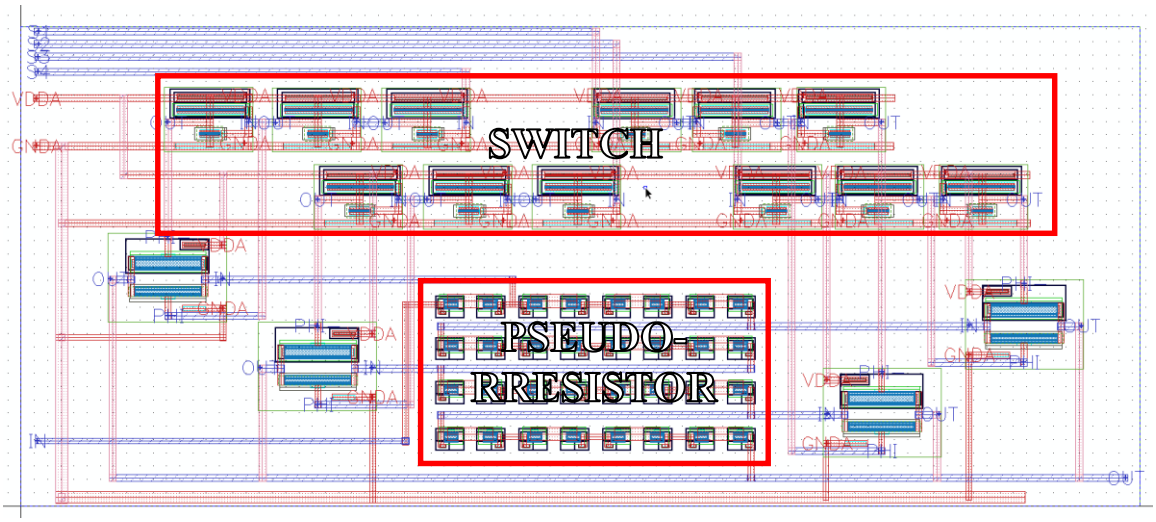

Figure 4.4 Layout of the pseudo resistor

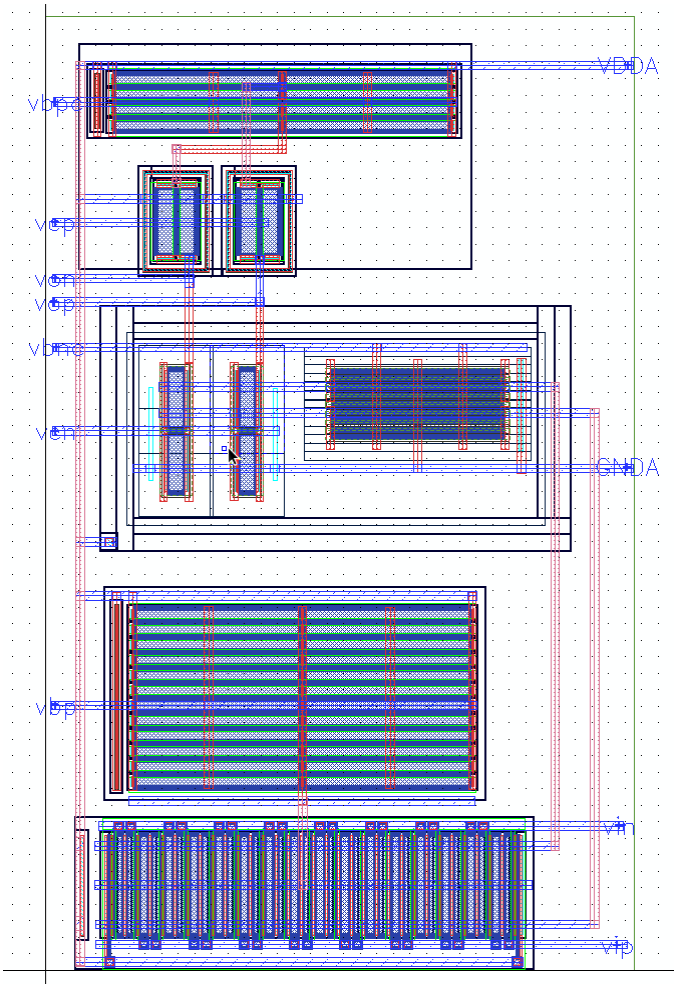

Figure 4.5 Layout of the fully differential amplifier

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For the electrical testing we needed to design a PCB which help us to do the test with different I/O case.

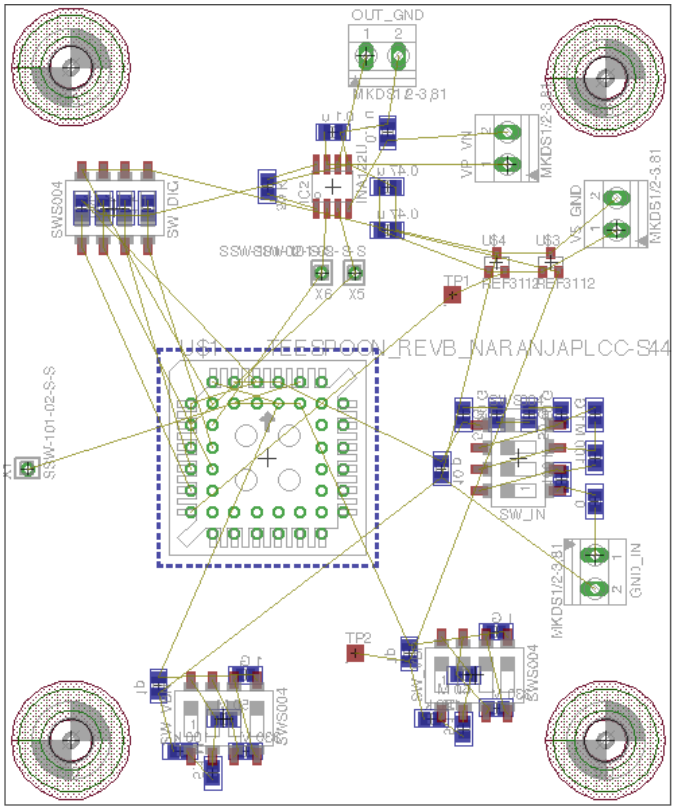

Figure 4.6 Layout of the test board

The measured parameters verified the usability of this architecture and show the advantages of the chained pseudo resistance, which provide the large time constant.

Due to the small frequency bandwidth of the bio-potential signals, it is the target noise level that defines the power dissipation of the bio-potential amplifiers. As the type and the number of noise sources increase, the total noise of the amplifier also increases. Therefore, the amplifier requires more power to achieve the target noise level.

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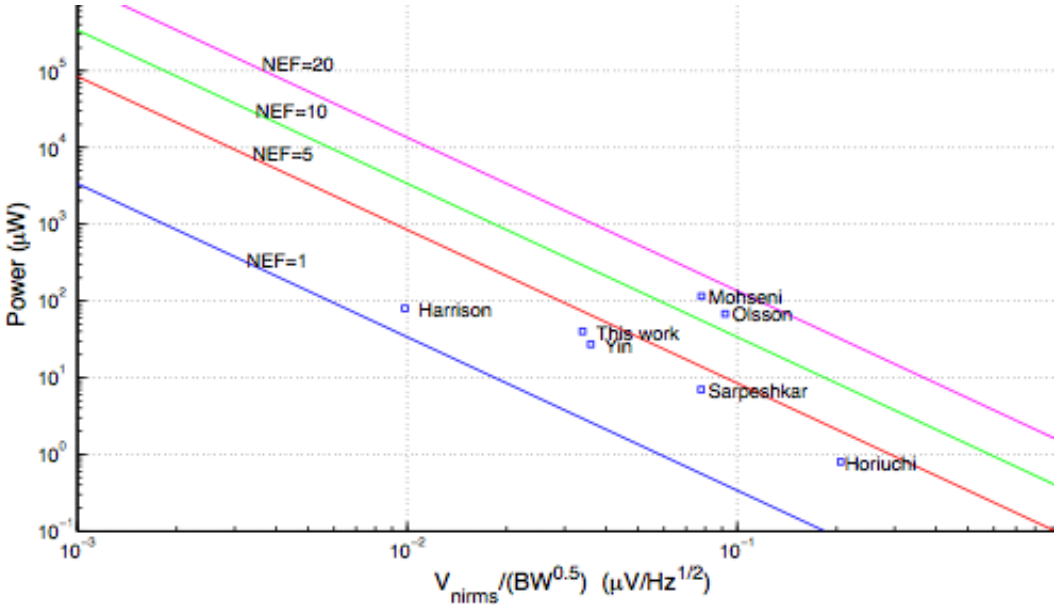

Figure 4.7 NEF comparison [7,17,33-36]

The in vivo experiments were approved by the Animal Care Committee of the Institute of Cognitive Neuroscience and Psychology, Research Centre for Natural Sciences, Hungarian Academy of Sciences, Budapest, Hungary. For the in vivo experiments we used Wistar rats (weight of 250-350 g, n = 3). Initial anesthesia was achieved by intramuscular injection of a mixture of 37.5 mg/ml ketamine and 5 mg/ml xylazine at 0.2 ml/100 g body weight. The temperature was maintained at 37 °C throughout the recording sessions. The anesthesia was maintained with several updates of the same drug at 0.2 ml/hour. Craniotomy was performed over the trunk region of the primary somatosensory cortex in a stereotaxic frame (David Kopf Instruments, Tujunga, CA). The target site was anterior-posterior -2.7 mm and medial-lateral 2.8 mm with respect to the bregma [17]. A silicon probe [18] was attached to a manual microdrive (David Kopf Instruments, Tujunga, CA) and it was slowly (0.1mm/sec) inserted in the trunk region. The amplifier was attached to the output leads of the silicon probe.

The outputs of the amplifier were fed into a high input impedance AD converter and digitized at 20 kHz/channel sampling rate, with 16-bit precision (PCI-6259, National Instruments, Austin, TX). The data was processed using NeuroScan Edit 4.3 software (Compumedics, El Paso, TX).

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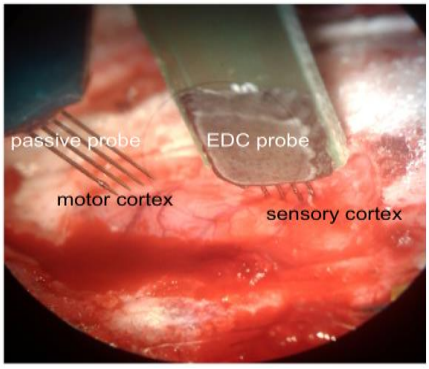

Figure 4.8 Picture about the probe insertion

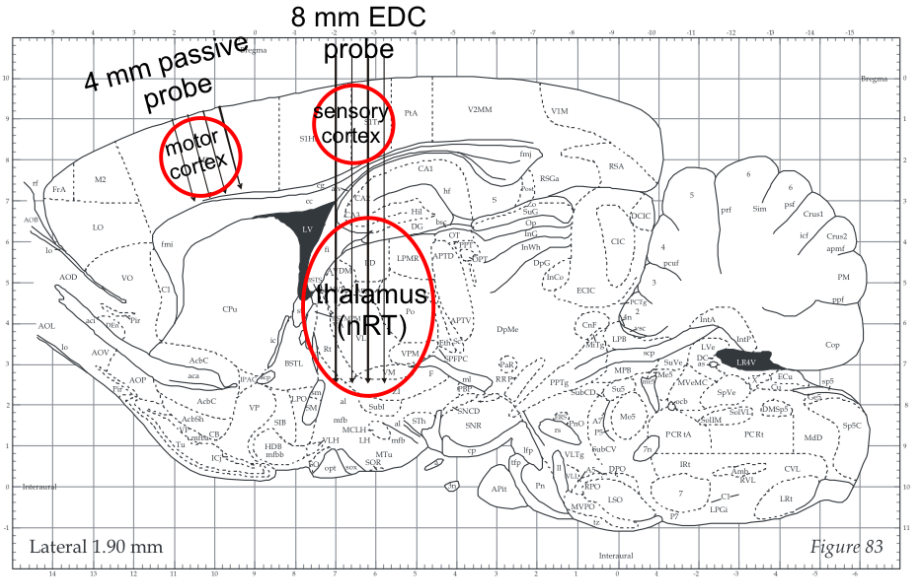

Figure 4.9 Schematic image about the probe positioning

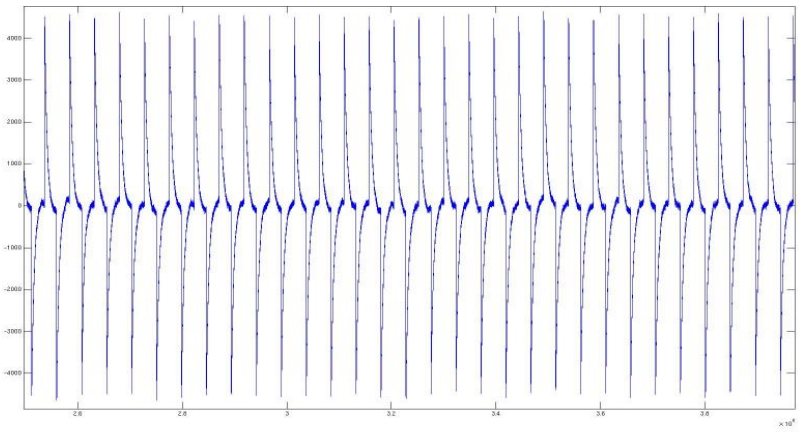

Figure. 4.10 Verification with EEG testing source

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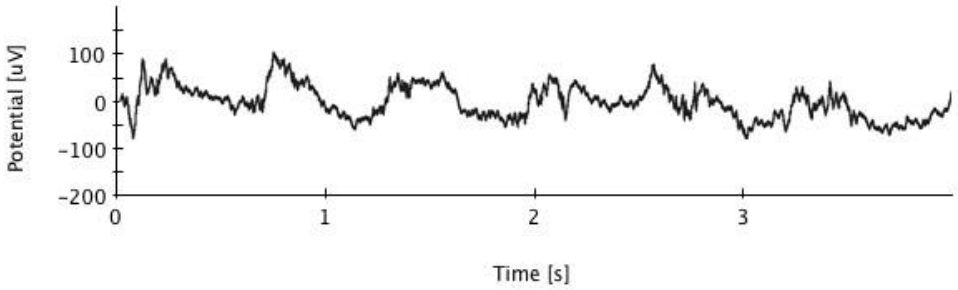

Figure 4.11.a Recorded LFP signal (2.8 – 500 Hz band-pass)

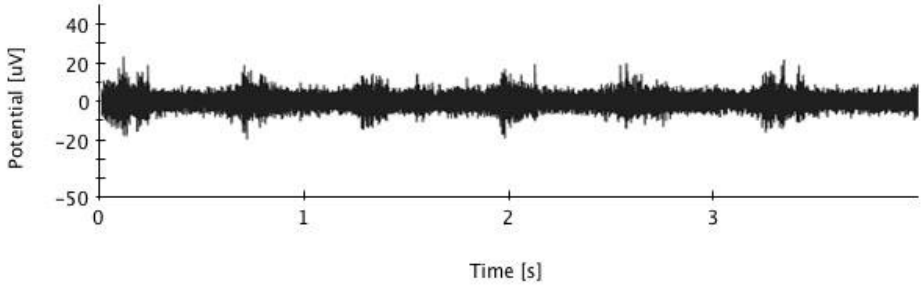

Figure 4.11.b Recorded MUA (500 Hz – 5 kHz band-pass)

As illustrated in figure 4.11, it was possible to record LFPs and MUA in the rat cortex. While the LFP is the summed synaptic activity of many neurons, the MUA shows the action potential firing of the cells close to the electrode contacts. Both signal types can be obtained from the raw data by filtering in the appropriate frequency range. Our results prove that the amplifier is functional in vivo.

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The main contribution in this work, the presented an integrated low noise amplifier circuit for the battery less implantable neural recording, and reviewed the most important design considerations. The MOS pseudo resistor chain is genuine innovation which is not used any other solutions on this area. The comparison between the switched-capacitance, the pseudo resistance and the modified OTA topologies as generally are not definite. As long as the current cancellation and division generate a continuously current consumption and not gives any chance for tuning the transfer-function [9], till then the switched capacitor provide a fine tuning method but generates high distortion [18]. The basic MOS pseudo resistance not able the handle the low frequency input, because the bad distortion and sensitivity for the corner variation as a SC resistance [29-33]. The gated chain could be the optimal solution. It gives the tuning range to decreasing the corner effect and to be able handle the local field potential range. In summary in this paper, an integrated tunable low noise amplifier circuit is presented for implantable neural recording, and introduced a MOS pseudo resistor chain outperforms existing solutions in terms of area and linearity.

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V. ULTRA-LOW NOISE AMPLIFIER

Any unwanted disturbances that obscure or interferes with a desired signal appear noise [24]. The thermal noise caused by the thermal agitation of charge carriers (electrons or holes) in a conductor. This noise is present in all passive resistive elements. Like shot noise, thermal noise is spectrally flat or has a uniform power density, but the thermal noise is independent of current flow. The total noise energy is limited by the effective capacitance across the terminals. *k* is Boltzmann's constant (1.38 × 10−23 j/K) Flicker was observed in vacuum tubes in a long period (only few cycle a day). The generation and recombination of carriers in surface energy states and density of surface state. Burst also called popcorn noise, appears to be related to imperfections in semiconductor material and heavy ion implants. Burst noise makes a popping sound at rates below 100 Hz when played through a speaker. Low burst noise is achieved by using clean device processing. Shot noise associated with current flow. Shot noise results whenever charges cross a potential barrier, like a pn junction. Crossing the potential barrier is a purely random event. Avalanche meaning when a pn junction is operated in the reverse breakdown mode. Under the influence of a strong reverse electric field within the junction's depletion region, electrons have enough kinetic energy that, when they collide with the atoms of the crystal lattice, additional electron-hole pairs are formed. Noise quantities can be added. Feedback cannot be used to reduce the equivalent noise of an op amp circuit.

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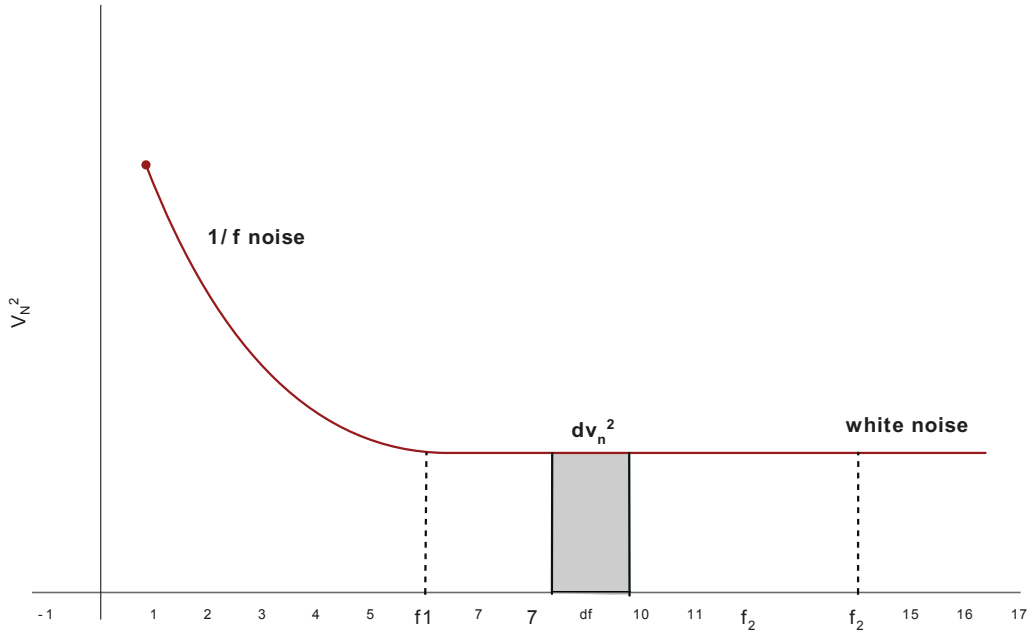

Figure 5.1 Noise distribution

Integrated noise can be calculated

$$V_{12} = \sqrt{V_N^2} = \sqrt{\int_{f1}^{f2} dV_N^2 df} \tag{5.1}$$

Noise analysis of different structures in an amplifier circuit:

A. *MOS transistor*

We can use the same model of p and n type transistors with every FET. A MOST has a resistive channel. It exhibits thermal noise, just like any other resistor. The channel noise can be represented by a noise current source in parallel with the g_m current source. The effective channel resistor R_{CH} of 2/3 g_m. The *4kT* factor clearly shows that we are dealing with thermal noise. The poly Gate resistor R_G cannot be discounted. Even if the Gate material is highly doped, it can make a large contribution, depending on the actual dimensions. The channel noise current can easily be shifted to the input by dividing it by g_m. The two noise powers are added at the input. In this way we obtain a thermal noise resistance R_{eff}, which is the sum of both sources. The channel noise gives the first contribution. The Gate resistor R_G is the other one. It is inversely proportional to transconductance, at least if the Gate resistor is small. A MOST device also exhibits a lot of *1/f* noise. The one with C_{ox2} in the denominator has the advantage, that

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coefficient KF is nearly independent of the technology. All technology effects are represented by the C_{ox2}. A MOST with a thin-oxide or a small channel length, and a large WL product shows little 1/f noise. We also note that a p-JFET is the transistor with lowest *1/f* noise [25]. A pMOST is about ten times worse. A nMOST is by far the worst transistor for *1/f* noise. It is 30–60 times larger than for a pMOST of the same size. It is for this reason that some audio preamplifiers still want JFETs at their inputs. This also applies to some radiation detection circuitry. The equivalent input 1/f noise voltage does not depend on the DC biasing current.

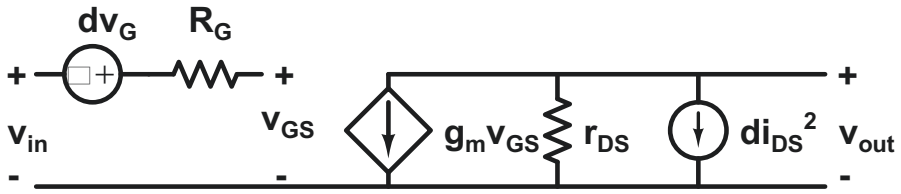

Figure 5.2 Small signal model for the thermal noise

$$dv_G = 4kTR_G df \tag{5.2}$$

$$di_{DS}{}^2 = \frac{4kT}{R_{CH}} df = 4kT\frac{2}{3} g_m df \tag{5.3}$$

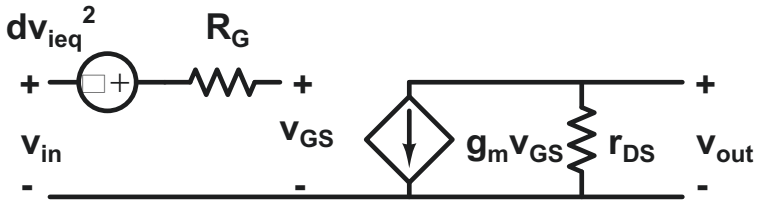

Figure 5.3 Small signal model for the input equivalent thermal noise

$$dv_{ieq}{}^2 = 4kT(R_{eff})df \tag{5.4}$$

$$R_{eff} = \frac{2/3}{g_m} + R_G \tag{5.5}$$

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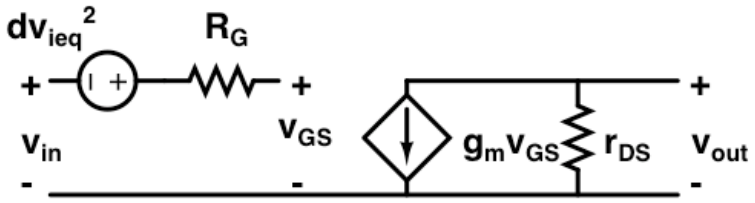

Figure 5.4 Small signal model for the equivalent flicker noise

$$dv_{ieqf}{}^2 = \frac{KF}{WLC_{ox}{}^2}\frac{df}{f} \tag{5.6}$$

$$pMOST\ KF \approx 10^{-32} C^2/cm^2$$

$$nMOST\ KF \approx 4\ 10^{-31} C^2/cm^2$$

$$pJFET\ KF \approx 10^{-33} C^2/cm^2$$

B. *Bipolar transistor*

A bipolar transistor has two pn-junctions, through which current flows. As a result, two sources of shot noise will have to be present white noise sources. One collector shot noise current source is added between collector and emitter. It is proportional to the collector current. The other one is between base and emitter and is proportional to the base current. Finally, a resistive base resistance noise voltage has to be added in series with the base input. Normally, the *1/f* noise is added to the base shot noise current source. The 1/f noise of a bipolar transistor is much lower than of a MOST because the current flows in the bulk, not at the surface. The 1/f noise is again inversely proportional to the emitter size A_{EB}. Again the noise sources can be combined at the input, in order to be able to compare them to the input signal. The collector shot noise has to be divided by g_{m2} in order to be translated into an input voltage. The base shot noise remains where it is. As a result, two equivalent noise sources are found, a voltage noise source and a current noise source, which is actually the base shot noise. The equivalent input noise voltage obviously also includes the base and emitter resistances. Note that the expression of the equivalent input voltage is very similar to the one for MOST. The only difference is that now the coefficient of $1/g_m$ is 1/2 instead of 2/3. This is small difference indeed. We cannot forget however that for the same DC

current the transconductance of a bipolar transistor is about 4 times larger than for a MOST. Its equivalent input noise voltage will therefore decrease.

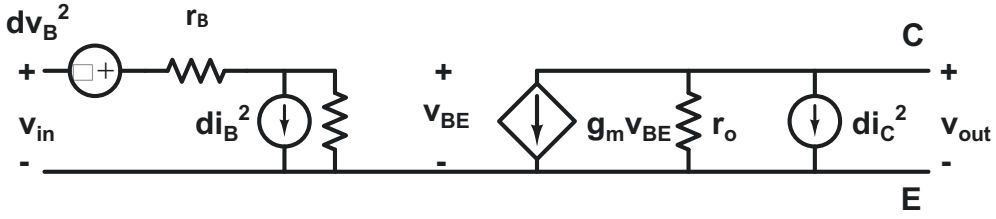

Figure 5.5 Small signal model for the thermal noise

$$dv_B{}^2 = 4kTr_B df \tag{5.7}$$

$$di_B{}^2 = 2qI_B df \tag{5.8}$$

$$di_C{}^2 = 2qI_C df \tag{5.9}$$

$$di_{Bf}{}^2 = \frac{KF_B I_B}{A_{EB}} \frac{df}{f} \tag{5.10}$$

$$KF_B \approx 10^{-21} Acm^2$$

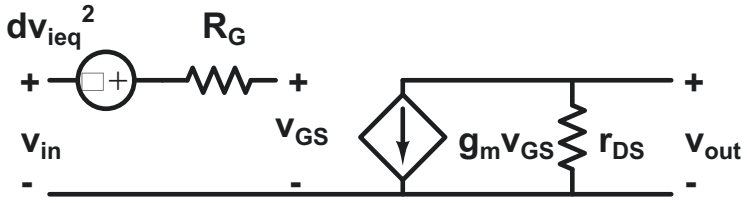

Figure 5.6 Small signal model for the equivalent flicker noise

$$dv_{ieq}{}^2 = 4kT(R_{eff})df \tag{5.11}$$

$$R_{eff} = \frac{1/2}{g_m} + R_B + R_E \tag{5.12}$$

$$di_{ieq}{}^2 = di_B = 2qI_B df \tag{5.13}$$

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C. *Noise with an active load*

The equivalent input noise source of the load transistor is shown explicitly. It is in series with the noise coming from the biasing voltage V_B. Normally this biasing voltage is followed by a large decoupling capacitance to ground, such that the noise from it can be ignored. The noise of the load transistor amplified by g_{m2} towards the output. It has to be divided by g_{m1} to be referred to the input. The noise of this transistor is therefore multiplied by a factor g_{m2}/g_{m1}. To make the noise contribution is negligible, we must design this load transistor with large $V_{GS}-V_T$ or small W/L. Both transistors now carry the same DC current. Transconductance g_{m2} can only be made smaller if it is designed for a larger $V_{GS}-V_T$, such as 0.5 V. The input transistor then keeps 0.2 V as a $V_{GS}-V_T$. This is an important conclusion, which will be repeated many times. Current source and current mirror devices must be designed for small size W/L and hence for large $V_{GS}-V_T$! Only the white noise sources have been considered here.

$$di_{out}^{\ 2} = g_{m1}^{\ 2} dv_1^{\ 2} + g_{m2}^{\ 2} dv_2^{\ 2} \tag{5.14}$$

$$dv_{ieq}^{\ 2} = dv_1^{\ 2} + dv_2^{\ 2} \left(\frac{g_{m2}}{g_{m1}}\right)^2 \tag{5.15}$$

$$dv_{ieq}^{\ 2} = dv_1^{\ 2} \left(1 + \frac{g_{m2}}{g_{m1}}\right) \tag{5.16}$$

The same analysis can be repeated for 1/f noise. However, all 1/f noise sources contain the area WL of the transistors. Moreover, the equivalent input noise voltage shows a minimum, if the input channel length is taken as a variable. It shows that the input transistor channel length must be about 10 times larger than load transistor channel length. This is not a problem as the load transistor has normally a small W/L. It is normally a small square device. The drawback could then be that the gain is reduced as a result of the small channel length. Cascodes will therefore be needed to alleviate this problem.

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D. *Differential pair*

The total equivalent input noise source is simply twice the noise voltage power of one single transistor. A differential amplifier always gives √2 more input noise voltage than a single amplifier [26]. The lowest-noise amplifiers are single-input. On the other hand, these single-input amplifiers are much more sensitive to substrate noise. The noise sources of all four transistors are added by their current sources. This is a circuit with two equal halves. If we know the input noise power for one halve, we simply multiply by two. Moreover, each half consists of an amplifying transistor loaded by a current source. To reduce the noise contribution of the current source: design larger $V_{GS}-V_T$. The resulting equivalent input voltage is now what we expected. It contains a factor of two for the two halves. Also it contains the g_m ratio, which is typical for an active load. If we succeed in making the load $V_{GS}-V_T$ small, then we can limit the input noise to the two input transistors only. However, if we choose the same $V_{GS}-V_T$ for all transistors or if we have bipolar transistors, then the noise of all 4 transistors is equally important.

The thermal and flicker noise models are briefly discussed, as they will prove useful in estimating the noise performance of the amplifier through hand calculations prior to simulation. The equation for thermal drain current noise that is used by the model and is appropriate for all bias points is

$$i_d^2 = \frac{4k_B\mu_{eff}Q_{inv}}{L^2}\Delta f \tag{5.17}$$

where k_B = Boltzmann's constant, T = temperature, μ_{eff} = effective channel mobility, Q_{inv} = channel charge and L = effective channel length

Q_{inv} can be expressed as

$$Q_{inv} = WLC_{ox}(V_{GS} - V_t)\frac{1-n+\frac{n^2}{3}}{1-\frac{n}{2}} \tag{5.18}$$

The thermal noise coefficient is defined as

$$\gamma = \frac{1-n+\frac{n^2}{3}}{1-\frac{n}{2}} \tag{5.19}$$

The values for γ in different regions of inversion have been presented in [27]. In weak inversion $\gamma = 1/2$ and in strong inversion, $\gamma = 2/3$.

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The drain-source conductance is given by

$$g_{ds} = \frac{\mu_{eff} Q_{inv}}{L^2} \tag{5.20}$$

Substituting the drain-source conductance from (5.20) in the expression for drain current noise in (6.17)

$$i_d^2 = 4k_B T \gamma g_{d0} \Delta f \tag{5.21}$$

Substituting the values of γ and neglecting body effect so that $g_{d0} = g_m$, we get

$$i_d^2 = 2k_B T g_m \Delta f \quad \text{weak inversion} \tag{5.22}$$

$$= \frac{8}{3} k_B T g_m \Delta f \quad \text{strong inversion} \tag{5.23}$$

This thermal noise current can now be reflected back to the gate in order to give the input-referred noise voltage ($v_g^2 = i_d^2/g_m^2$) as

$$v_{gT}^2 = \frac{2k_B T}{g_m} \Delta f \quad \text{weak inversion} \tag{5.24}$$

$$= \frac{8k_B T}{3g_m} \Delta f \quad \text{strong inversion} \tag{5.25}$$

This equivalent noise voltage source will be used to determine equivalent amplifier input-referred noise. In order to minimize the noise voltage at the gate for a given drain current, the subthreshold region of operation is preferred to the strong inversion region.

Noise models for 1/f noise in different regions of operation have been provided in [28] and measured results have been correlated to noise models used by the SPECTRE simulators. The drain noise current is given

$$i_d^2 = \frac{KF_{WI} {I_d}^2}{C_{ox} W L f} \Delta f \quad \text{weak inversion} \tag{5.26}$$

$$= \frac{KF_{SI} I_d}{C_{ox} W L^2 f} \Delta f \quad \text{strong inversion} \tag{5.27}$$

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It must be noted that KF has different values in the weak inversion and strong inversion regions. We must reflect this noisy drain current back to the gate to obtain the input-referred noise voltage, similar to the operation carried out for thermal noise. The gate transconductance in each region of operation is given by

$$g_m = \frac{\kappa I_d}{V_T} \quad \text{weak inversion} \tag{5.28}$$

$$= \sqrt{2 I_d \mu C_{ox} \frac{W}{L}} \quad \text{strong inversion} \tag{5.29}$$

V_T is the thermal voltage kT/q and κ is the subthreshold gate coupling coefficient and has a typical value of 0.7. The expression for g_m in the subthreshold region is obtained from the EKV model [29] and will be explained while considering amplifier design. Using the values of g_m from (5.28) and (5.29) in order to reflect the flicker noise current back to the gate, we get

$$v_{g_{1/f}}^2 = \frac{KF_{WI} {V_T}^2}{\kappa^2 C_{ox} W L f} \Delta f \quad \text{weak inversion} \tag{5.30}$$

$$= \frac{KF_{SI}}{2\mu C_{ox} W L f} \Delta f \quad \text{strong inversion} \tag{5.31}$$

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E. *Differential Noise factor versus power consumption*

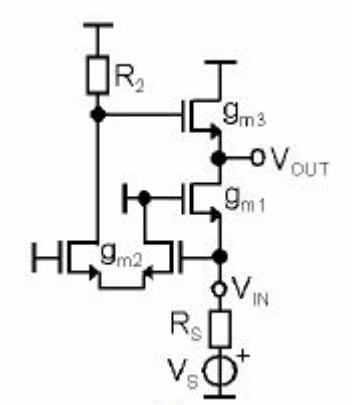

Figure 5.7 Alternative implementations of a noise-cancelling amplifier

The noise factor of different amplifiers is compared assuming power consumption (and not $g_{m2}R_S$) as independent variable. This is because:

- Low power is an important requirement in many systems. In battery-operated systems, low power preserves battery lifetime. Next, it enables the use of a low-cost IC package.

- Generally, wide-band LNAs provide a lower F at larger power levels. Fixing the power budget, topologies that are inherently capable of lower F are then highlighted. Neglecting the small contribution of the biasing circuitry, the power consumption P of the amplifier in figure 5.7 can be written as:

$$P = \frac{V_{DD}}{R_S} \sum_i g_{m,i} R_S \left(\frac{I_i}{g_{m,i}} \right) \tag{5.32}$$

where g_{mi} and $g_{m,i}/I_i$ are the transconductance and the g_m-efficiency of the transconductor implementing the VCCS (e.g.: MOST differential pair) and V_{DD} is the supply voltage. In equation (5.32), the sum is extended to the VCCSs determining the power of the amplifiers in figure 5.7 (i.e. g_{m1}, g_{m2} and eventually g_{m3}). Equation can be written as:

$$P = \frac{V_{DD}}{R_S} \sum_i \frac{g_{m,i} R_S}{\xi_i} \left(\frac{I_{D,i}}{g_{m,i}} \right)_{MOST,CS} \tag{5.33}$$

The efficiency factor, $\xi_i > 0$, is used to relate the efficiency of a transconductor to that of a common-source (CS) MOST, $(g_{m,i}/I_{D,i})_{MOST,CS}$, which is chosen as reference. Assuming equal $(g_{m,i}/I_{D,i})_{MOST,CS}$ (i.e. optimal power efficiency), equation (5.33) yields to:

$$P = P_{MOST,CS}\, \eta_{LNA} \tag{5.34}$$

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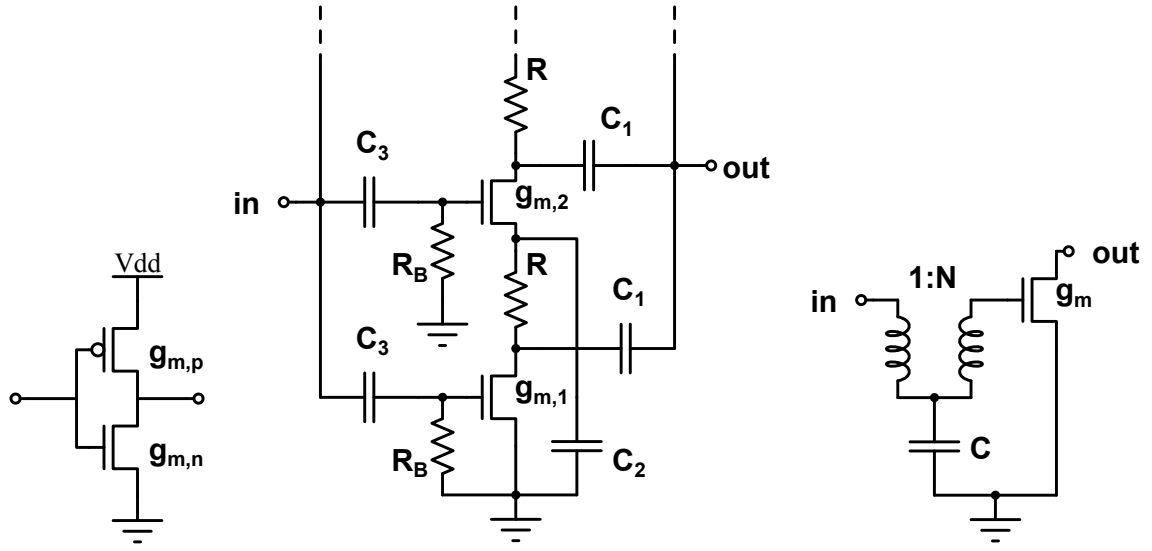
$$P_{MOST,CS} = \frac{V_{DD}}{R_S}\left(\frac{I_D}{g_m}\right)_{MOST,CS} \tag{5.35}$$

$$\eta_{LNA} = \sum_i \frac{g_{m,i}R_S}{\xi_i} \tag{5.36}$$

Equation (5.34) shows that the power consumption of the noise-cancelling amplifiers is the product of the (reference) power consumption $P_{MOST,CS}$ of a CS MOST with $g_m=1/R_S$ and given g_m/I_D (as the other VCCS circuits in the amplifier) multiplied by the normalized power factor $\eta_{LNA}=(P/P_{MOST,CS})$. The latter is circuit-dependent through the sum of $g_{m,i}R_S$ and the efficiency factor ξi. We now look at ways to enhance the efficiency factor ξ of a transconductor. Figure 5.8 shows some transconductor circuits providing a larger ξ.



a) b) c)

Figure 5.8: Transconductor circuits with improved efficiency factor ξ by exploiting: a)-b) MOST bias current re-use and c) Wide-band 1:N step-up transformer.

Circuits a) and b) achieve a larger ξ re-using the bias-current of another MOST. The g_m/I of the inverter in figure 7.8a is:

$$\frac{g_m}{I} = \frac{g_{m,n}}{I_D}\left(1+\frac{g_{m,p}}{g_{m,n}}\right) \approx \frac{g_{m,n}}{I_D}\left(1+\sqrt{\frac{K_pW_p}{K_nW_n}}\right) = \frac{g_{m,n}}{I_D}\xi \tag{5.37}$$

where $K_{n(p)}=\mu_{n(p)}C_{ox,n(p)}$ and $L_p=L_n$ were assumed. Fixed $g_{m,n}/I_D$ and W_n (and so I_D), the inverter efficiency factor ξ is larger than 1. For $W_p=W_nK_n/K_p$, ξ is 2. This means that the g_m of an inverter is 2

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times $g_{m,n}$ for the same bias I_D. For a typical CMOS process, K_n is about 2-3 times K_p. This requires large PMOST, which increases input capacitance C_{IN} as:

$$C_{IN} = C_{gs,n} + C_{gs,p} \approx C_{gs,n}\left(1 + \frac{W_p}{W_n}\right) \tag{5.38}$$

and $C_{ox,n}=C_{ox,p}$ was used. For $W_p=W_n\mu_n/\mu_p$, the excess of input capacitance. $C_{gs,n}(\mu_n/\mu_p-1)$, can be substantial (e.g.: 2 or 3 times $C_{gs,n}$). Next, for a fixed bias current, the g_m/I of the inverter increases as the square root of W_p, while C_{IN} increases linearly with W_p. Thus, the inverter unity-gain cut-off frequency, $f_T=g_m/(2\pi C_{IN})$, drops as the inverse of the square root of W_p. To mitigate the previous problems, the circuit in figure 5.8b may be used. Here, the bias current of the bottom NMOST is re-used by a MOST of the same type. The total g_m approaches then the sum of the g_m of the stacked MOSTs (i.e. ξ = number of stacked MOSTs). Nevertheless, this solution requires extra resistors, capacitors and dc sources to bias correctly the MOSTs and ground their source terminals. These components increase chip-area and introduce bandwidth limitations. Moreover, the output noise of R may be not negligible. These issues impair at a low supply-voltage, due to the insufficient voltage headroom available for the stacked MOSTs and R's. Figure 5.8c shows an alternative approach. A step-up 1:N transformer in front of a MOST boosts the g_m to $N \cdot g_m$ ($\xi = N$). Unfortunately, wide-band transformers of acceptable performance are difficult to integrate, especially in CMOS.

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VI. CMOS AND BI-CMOS ULTRA LOW NOISE AMPLIFIER ARRAY FOR BRAIN SIGNAL MEASUREMENT

Recording neural activity has become important for basic research in neuroscience [1]. Minimizing the noise and assure the sufficient distortion in a bio-signal recording application was the key element in this design. While the energy consumption and the area usage was not a hard constraint within the rational cost range. The amplifier is the first stage in an in-vivo experiment. It was designed especially for our purpose to get an amplified signal with minimum noise and distortion from the electrodes with compact sized equipment. The amplifier placed outside of the cerebellum. The electrode shaft has 24 recording sites and 16 can be select at the same time. The circuit is presented below (Fig. 6.1) is able to amplify those signals with the possibly smallest noise and distortion. Because of this module was not implanted therefore the specification could be changed, so the current consumption and related thermal dissipation was not so strict restriction as it would be otherwise.

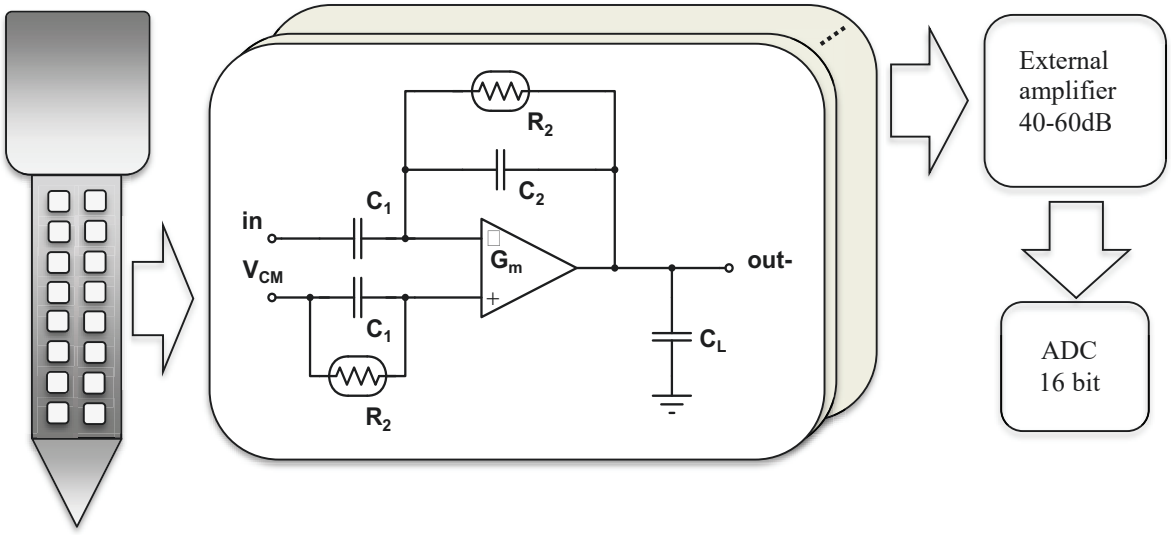

Figure 6.1 Electrode shaft with 16 sites connecting to the LNA matrix

To achieve the specification noise criteria and get less than 1μV/√(Hz), it was necessary to do a comparison between the different technologies and architectures [2-3]. The amplifier had to be working in both the local field potential and the action potential range. In ordered to get the most usable signal

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the recording of the sub-hertz frequency was also necessary. To get a long time constant amplifier we used MOS pseudo-resistors. To avoiding the drawback of this solution, like the increased distortion, a chained series of these elements was used. It is inevitable to optimizing size and the number of the transistors in the chain, because increasing the number of element lead to decreasing the distortion and increasing the noise at same time. In chapter III the Figure 3.6 illustrate a basic design flow for the optimization. The used technology also specifies the limitation of the circuit. After the analyzing of the noise correspondence in different solution at the literature [4-7] we decided the keep the circuit as simple as it possible to realize the smallest noise, that is shown in figure 6.2 and the small signal model in 6.3.

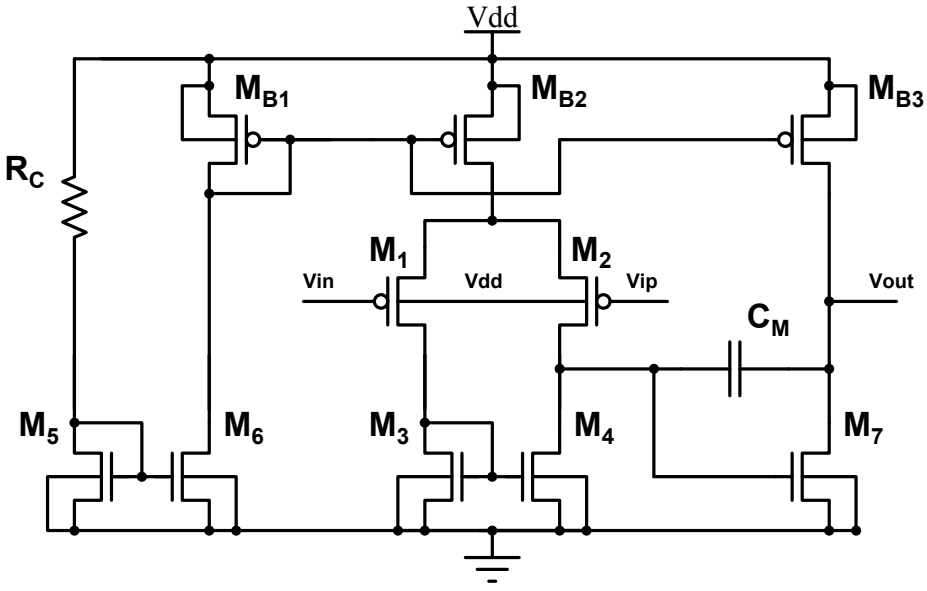

Figure 6.2 Schematic for the CMOS OTA

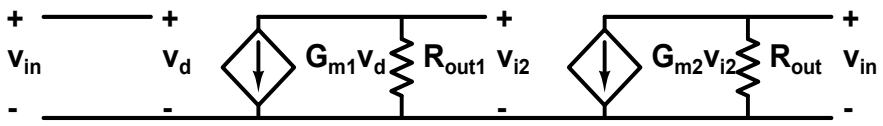

Figure 6.3 Small signal model for the OTA

The $M_{1\text{-}2}$ is the input transistor and $M_{3\text{-}4}$ is the loading transistors. M_{Bx} are corresponding for the biasing and C_M for the Miller compensation. The flicker noise is a general problem in a low frequency recording especially in LFP range. Over 100 Hz the thermal noise will be significant. To attenuate the noise, we examined the both the available CMOS and BiCMOS technologies. The bipolar transistors

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generate less flicker noise. Unfortunately, the input resistors which has the largest impact in the noise have to be MOS type to get high input resistance. Commute only the loading MOS transistors with bipolar ones was not been enough. It was necessary to add another stage to avoid the reduced low-frequency gain by increasing the input resistance of the second stage. The original amplification can be calculated:

$$a_{vdo} = g_{m1}(r_{o2}||r_{o4}||r_{\pi 7})g_{m7}(r_{o7}||r_{ob3}) \tag{6.1}$$

If we exchange the load transistors (M_3, M_4, M_7) than

$$r_{o2}, r_{o4} << r_{\pi 7} \tag{6.2}$$

$$a_{vdo} \approx g_{m1} r_{\pi 7}\, g_{m7}(r_{o7}||r_{ob3}) \tag{6.3}$$

would be degraded. The BiCMOS solution gives higher unity gain and lower flicker noise, beside it occupies more area and it worse in thermal noise. The size of the used instances can be seen on Table 6.1.

Element	**CMOS LNA**	**Bi-CMOS LNA**
M_1/M_2	2100/1	2100/1
M_3/M_4	250/19	-
M_5	113/3	113/3
M_6	2/3	2/3
M_7	100/19	12/3
M_8	-	12/3
MB_1	19/1	19/1
MB_2	1729/1	1729/1
MB_3	57/1	19/1
MB_4	-	57/1
Q_1-Q_6	-	96
R_C	18 kΩ	18 kΩ
C_M	60 pF	180 pF

Table. 6.1 Transistor size chart, W/L dimensions in μm

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In order to design the lowest noise amplifier, it was needful to optimize the layout using interleaving, common centroid techniques and dummy transistors with precaution on symmetric placing and routing. For the larger size transistors with multiple fingers using the common centroid eventually rule higher noise. After the parasitic extraction the simulations indicated with the CMOS solution would guarantee better parameters. The experiments confirmed the results of the simulation. Using the same size of amplifiers, the CMOS solution generate lower noise. The chip was built with the AMS 0.35µm BiCMOS technology. The layout of the CMOS amplifier can be seen on figure 6.4. The whole layout is presented on figure 6.7, while the die photo is on figure 6.8.

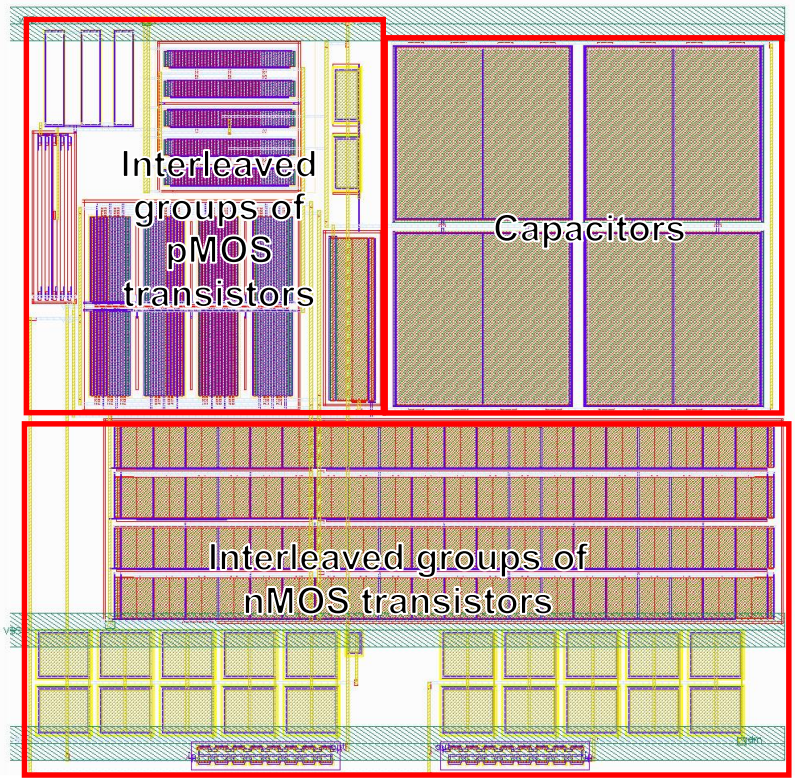

Figure 6.4 Layout for the CMOS OTA

In order to exploit the advantages of the BiCMOS technology it was necessary to use an additional stage in the amplifier to stabilize the output gain. It can be seen of figure 6.5.

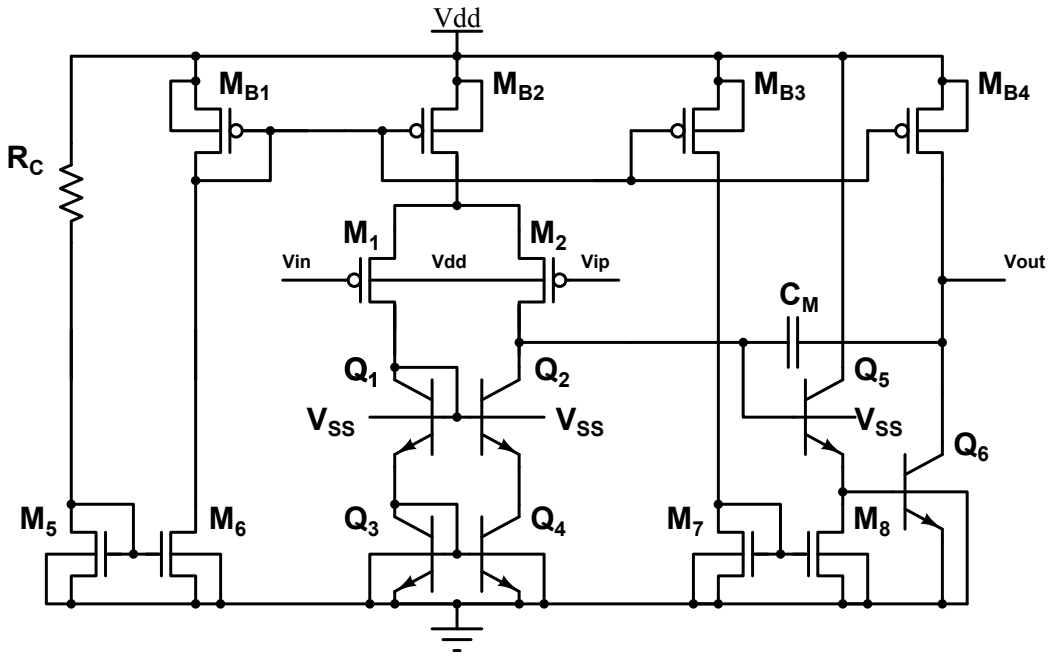

Figure 6.5 Schematic of the Bi-CMOS OTA

The comparison between the CMOS and BiCMOS amplifier gives us the chance to decide which technology imply greater advantages over this type of animal studies. After finishing the layout, we can do the post layout noise simulation (Fig. 6.6).

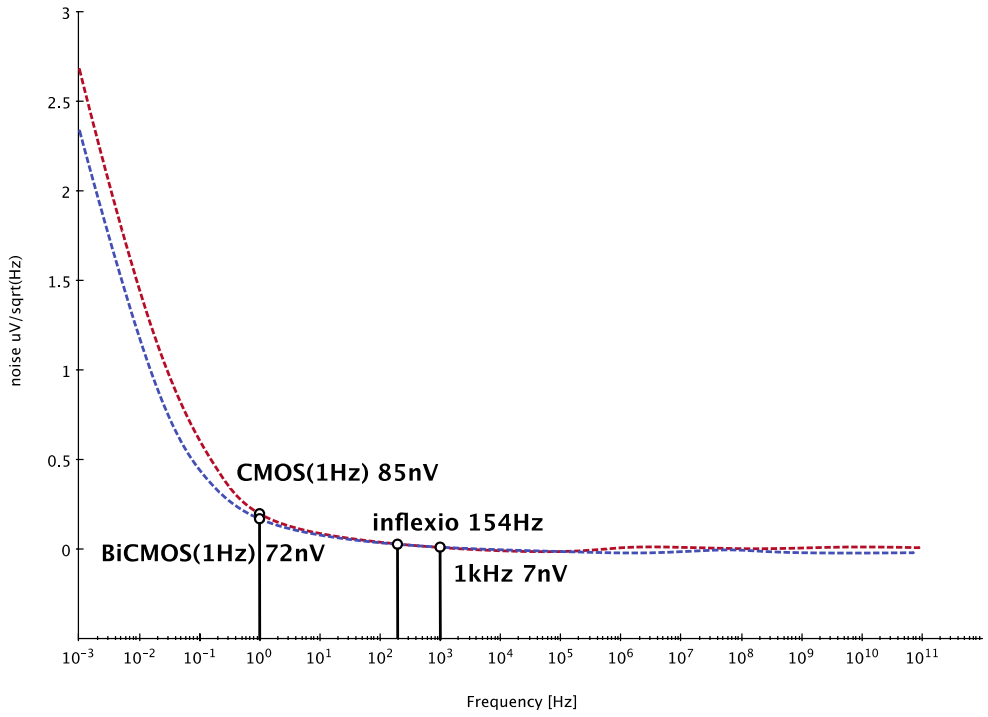

Figure 6.6 The difference in post layout noise simulation between BiCMOS and CMOS

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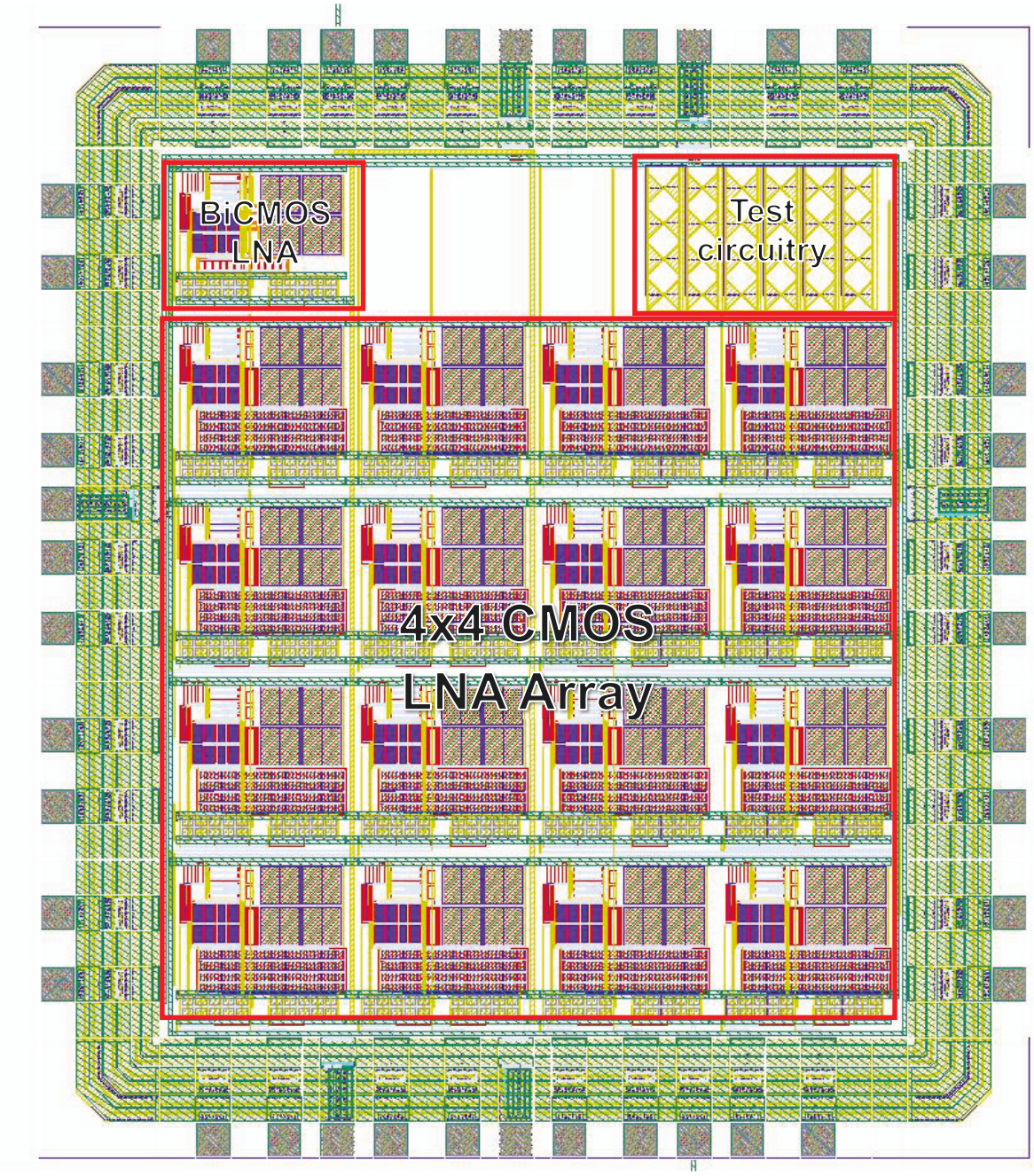

Figure 6.7 Layout for the LNA matrix

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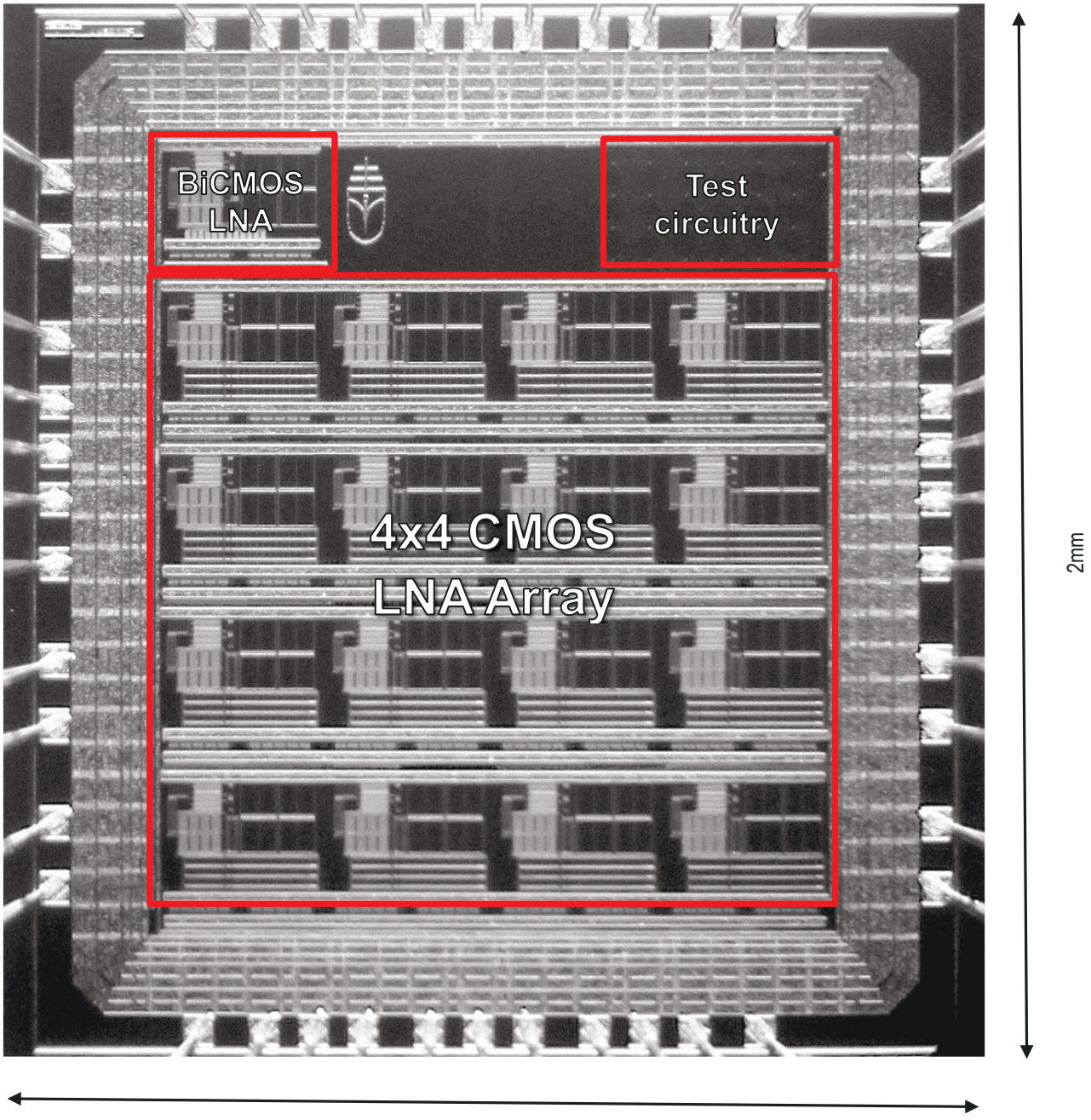

Figure 6.8 Die Photo of the bonded chip (AMS .35 Bi-CMOS)

The laboratory setup can be seen on figure 6.9 and the received LFP on figure 6.10. The amplifier inputs connect directly to the neural probe, while the outputs connect to a distant external amplifier through 5m cable. The standard deviation of the gain at the CMOS amplifier was 0.33dB and 0.26dB at the BiCMOS.

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Figure 6.9 Photo about the in-vivo testing in a rodent experiment

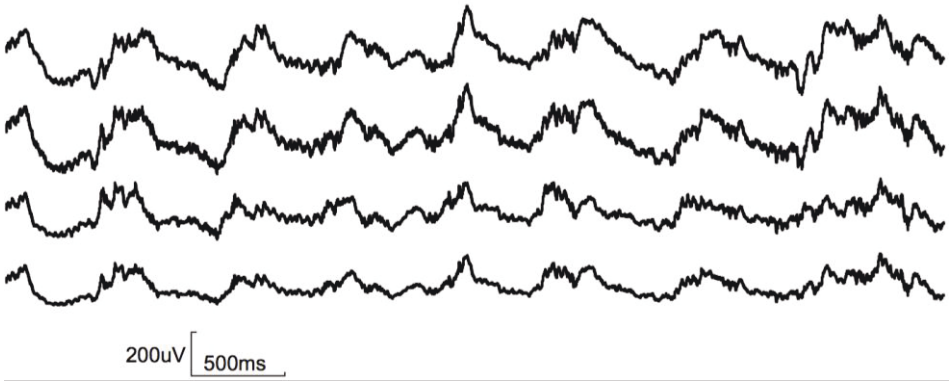

Figure 6.10: Recorded LFP signals

In conclusion, we implemented an ultralow noise CMOS and BiCMOS amplifier, which can be connected to neural probe. The figure 6.11. and table 6.2 shows the simulated and measured parameters for both types of amplifiers. The measured input referred noise was 670nV/√(Hz) with 22mHz cutoff frequency for the CMOS amplifier which is exceed our prior expectation.

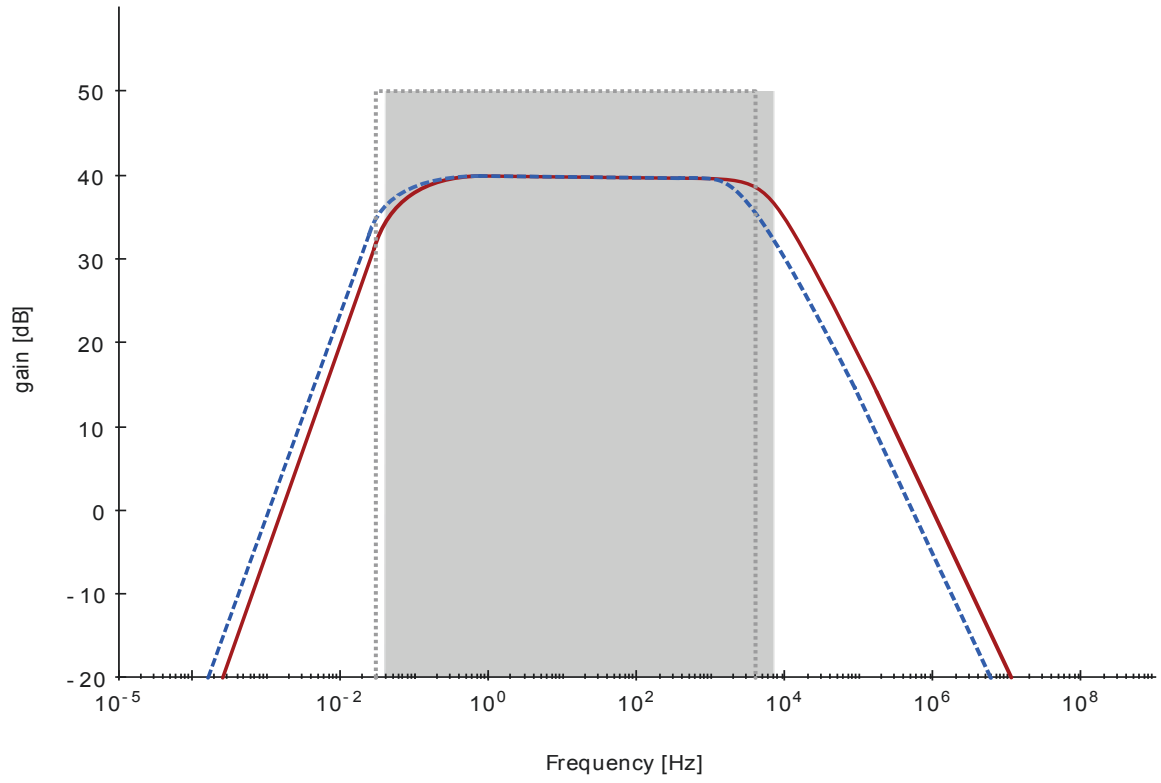

Figure 6.11 The simulated (red) and measured (blue) transfer characteristic

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Parameter	**CMOS LNA**	**Bi-CMOS LNA**
Supply Voltage	1.6 V	1.6 V
Process Technology	0.35 μm Bi-CMOS	0.35 μm Bi-CMOS
Midband Gain	40 dB	40 dB
-3 dB Bandwidth	53 (22) mHz ~ 10 (6) kHz	55 (30) mHz ~ 9.8 (6.5) kHz
Input Referred Noise	610 (670) nV_{rms}	777 (860) nV_{rms}
Noise Efficiency Factor	4.4	4.2
THD	-90 dB	-94 dB
CMRR	39.6 dB	37.5 dB
PSRR	75.8 dB	77.2 dB
ICMR	2.36 V	1.92 V
Slew rate (1 mV input)	1.3 mV/μs	1.5 mV/μs
Power Consumption	240 μW	220 μW

Table 6.2: simulated and measured (in brackets) parameters of the CMOS and BiCMOS LNA

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VII. NEURO PROBE DESIGN

In the last section I'll present one of the most advanced neuro probe in 2015, which designed by a research team where I was working in IMEC Belgium. My role in this project was to design reusable filter and low noise amplifier blocks before the analog digital conversion. It is further practical evidence, my thesis's are valuable and useful in bio-signal recording tasks.

This advanced neuro probe includes 1424 recording sites. This solution with the higher density than any previous before can provide better performance than existing technology by an order of magnitude. This will allow researchers to record brain activity with an unprecedented combination of resolution and a very large number of sites. The sensors under development have the potential to enable transformational neurobiology experiments and to contribute to a fundamentally improved understanding of how neurons in the brain work together to process information and control behavior.

	Name	**LFP Band**	**AP Band**
Electrical	Noise from a single site.	50 µVrms	10 µVrms
	BW	< 1 Hz – 1kHz (adjustable)	0.2 kHz – 7.6 kHz (adjustable)
	Gain	Adjustable (200-2000)	Adjustable
	Sampling rate	20kHz	2kHz
	Resolution	10bit	
	Crosstalk	<5%	
	Electrode impedance/fidelity	One electrode at a time (before measurements).	
	Data transfer rate	384Mbps (data might need additional error correction bit)	
Structural	Probe length	8 mm	
	Probe width	100 µm	
	Probe thickness	50 µm	
	Electrode size	20 x 20 μm^2	
	Number of readout electrodes	1424	

Table 7.1 Specification for the neuro probe design

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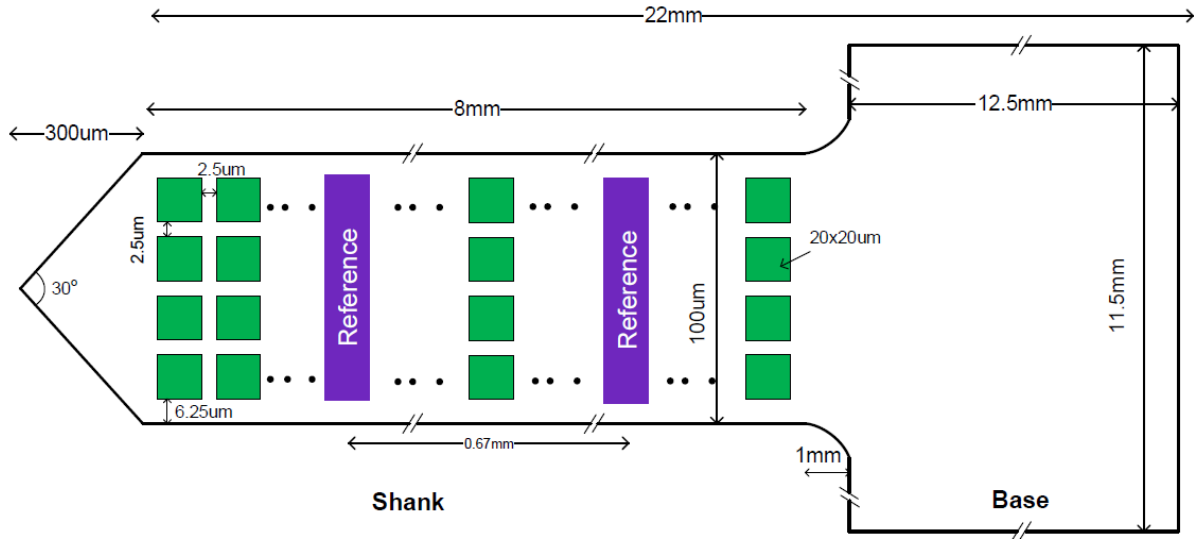

Figure 7.1 Schematic about the shank with the sites location

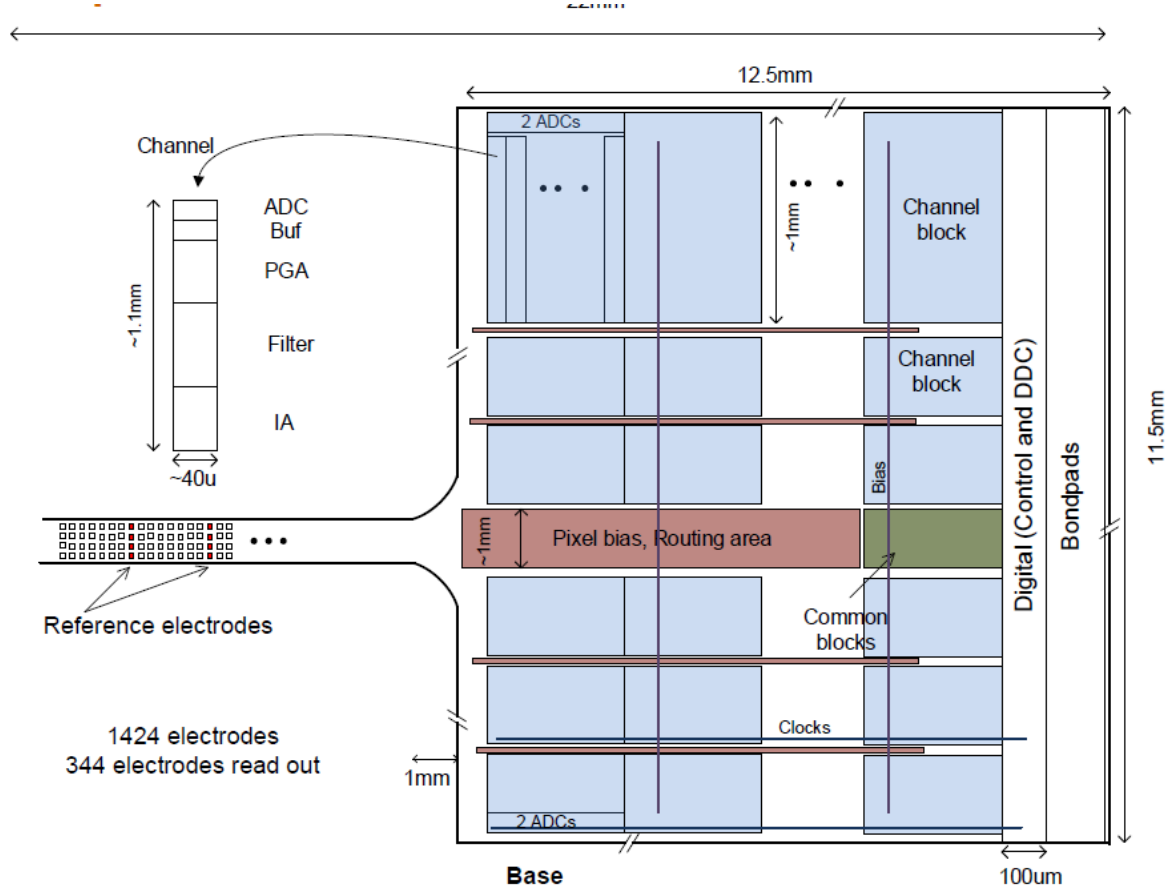

Figure 7.2 Overview about the base architecture

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Thermal simulation with the Comsol Multiphysics software can be seen on figure 7.3. Using the semiconductor module, we were able to compute the non-isothermal transport simulation which are based on drift-diffusion equations. With those results we could give a good approximation about the maximum allowed dissipation on the shank to avoid the brain tissue damage.

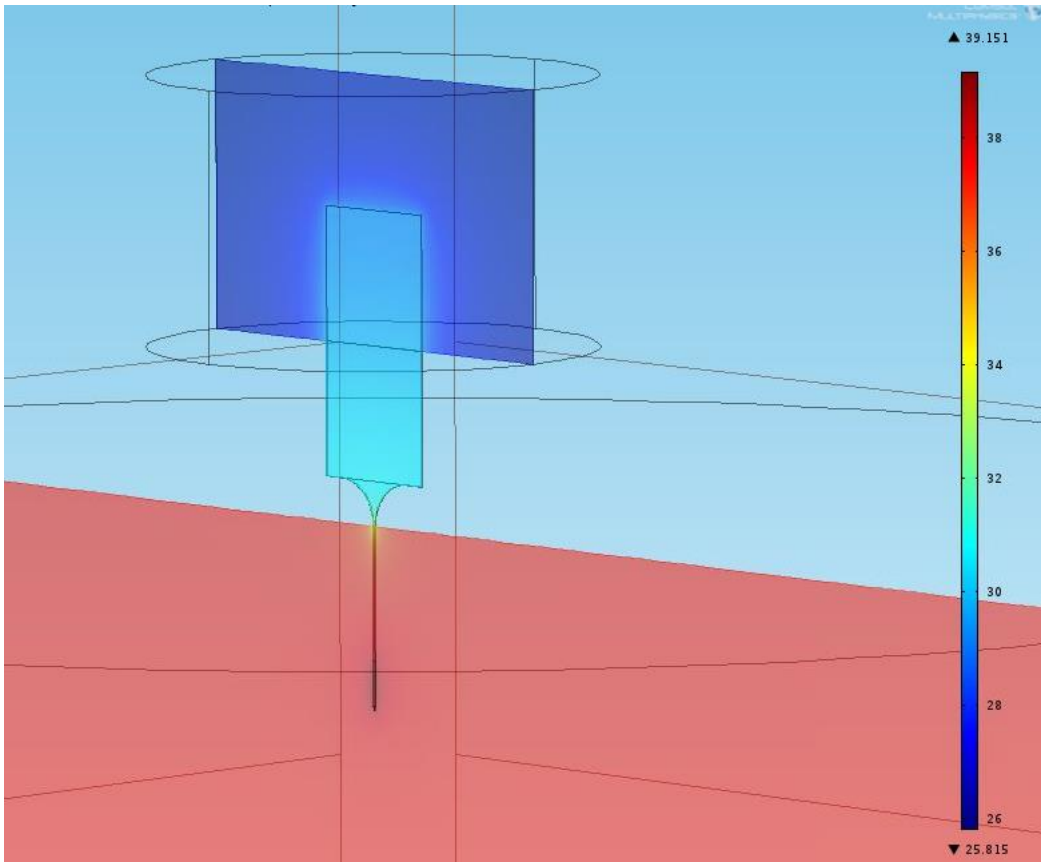

Figure 7.3 Thermal simulation on the implanted shank

Filter Design

In order to implement a filter, we could choose between active and passive architectures. To compare them we examined the size, noise and power consumption parameters. We choose a unity-gain Sallen-Key active low-pass filter topology. These circuit are suitable for filter which has complex conjugate poles. the unity-gain topology in figure 7.4. This architecture is usually applied in filter designs with high gain accuracy, unity gain, and low Q_s ($Q < 3$).

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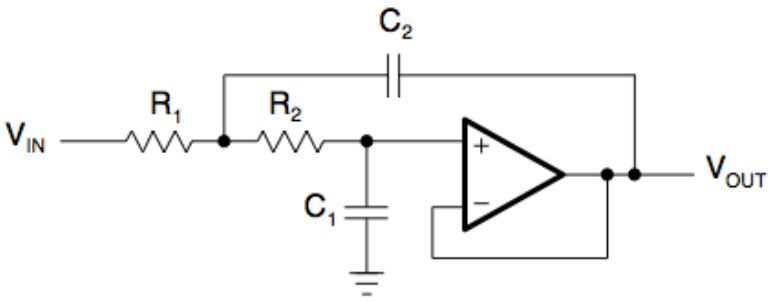

Figure 7.4 Unity-Gain Sallen-Key Active Low-Pass Filter

Transfer function for this topology can be calculated:

$$A(s) = \frac{1}{1+\omega_c C_1(R_1+R_2)s+\omega_c{}^2 C_1 C_2 R_1 R_2 s^2} \tag{7.1}$$

where the coefficients:

$$a_1 = \omega_c C_1(R_1 + R_2) \tag{7.2}$$

$$b_1 = \omega_c{}^2 C_1 C_2 R_1 R_2 \tag{7.3}$$

Resistor calculation:

$$R_{1,2} = \frac{a_1 C_2 \pm \sqrt{a_1{}^2 C_2{}^2 - 4 b_1 C_1 C_2}}{4\pi f_c C_1 C_2} \tag{7.4}$$

In order to obtain real values under the square root, C_2 must satisfy the following condition:

$$C_2 \geq C_1 \frac{4b_1}{a_1{}^2} \tag{7.5}$$

The task specification determined low pass corner frequency and the filter has to be 2nd order which gave the following values:

f_c = 1 kHz

a_1 = 1.065

b_1 = 1.905

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Using the equations 7.4 and 7.5, we can determine the capacitance and resistance values in the circuit.

C_1 = 104 fF

C_2 = 705 fF

R_1 = 79.4 MΩ

R_2 = 84.4 MΩ

Small size LNA OTA design

The used topology basically a two-stage Operation Transconductance Amplifier (OTA). The OTA is an amplifier which output current is a proportional to the differential input voltage. It is an Operational amplifier without the output buffer. Usually preferred over the op-amps because their simplicity and size advantage. OTAs can be classified into folded cascode and telescopic architectures. In this design we used a folded cascode topology (Fig. 7.5).

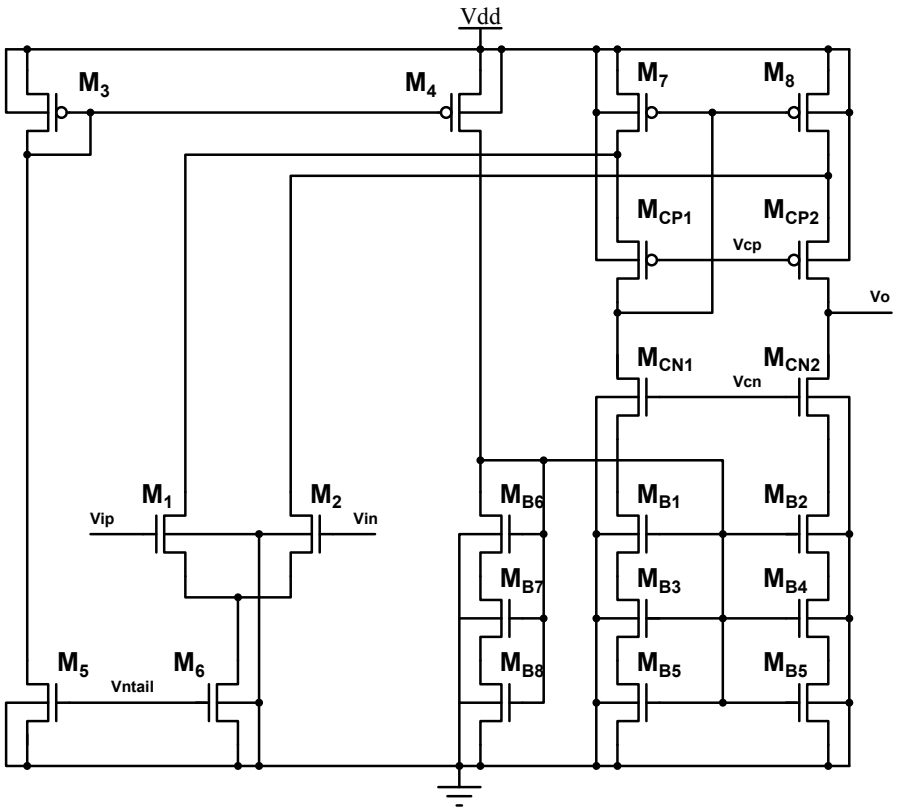

Figure 7.5 Folded cascode OTA schematic

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The used transistor size can be seen in Table 7.2.

Element	**CMOS LNA**
M_1/M_2	24/0.5
M_3	4/40
M_4	4/1
M_5	1/10
M_6	1/140
M_7/M_8	4/15
$M_{CP1}/M_{CP2}/M_{CN1}/M_{CN2}$	10/0.13
M_{CN1}/M_{CN2}	10/0.13
MB_1-MB_6	1/60
MB_7-MB_9	1/10

Table 7.2 Transistor size chart, W/L dimensions in μm

Switched capacitor as resistor

Simple SCR can be used as a tunable active resistance element. The role of the resistor is to take a certain amount of charge between two nodes in the circuit. We can perform the same function by a capacitor. The SC operates as a discrete-time equivalent resistor.

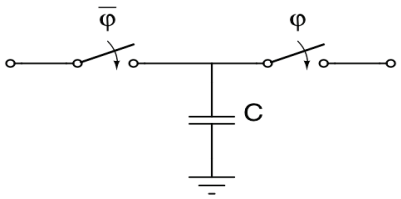

Figure 7.6 Simple SCR

$$I = qf = C(V_{OUT} - V_{IN})f \tag{7.6}$$

$$V = V_{OUT} - V_{IN} \tag{7.7}$$

$$R = \frac{V}{I} = \frac{1}{Cf} \tag{7.8}$$

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Improved SCR

In order to improve the capacity and improve the equivalent resistance we can modify the basic SC element. Using a two phase control signal and the following architecture (Fig. 7.7), the resistance will be increasing by 10 times compared to the original scheme.

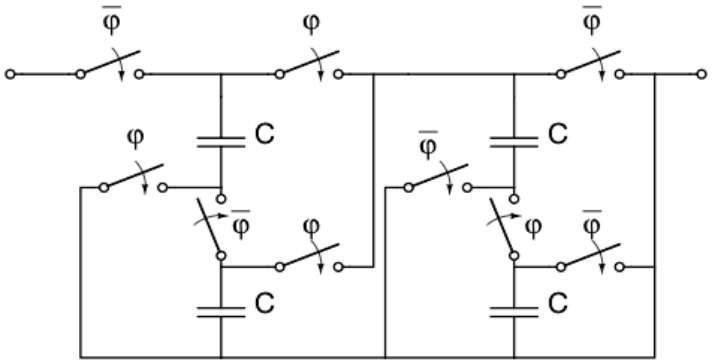

Figure 7.7 Improved SCR

$$R = \frac{10}{cf} \tag{7.9}$$

Comparison between simple and improved SCR:

Increase cap: + less noise

- parallel with C_2 (lower A_M)

Decrease cap: + higher resistance

- higher noise

- parasitic cap effect

- mismatch

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The schematic of the passive filter implementation with tunability can be seen on figure 7.8, while the layout of this same circuit on figure 7.9. Due to the requirements of the reusability and modularity, every element in the circuit have fixed width parameter. It helps to place each element with minimal overhead.

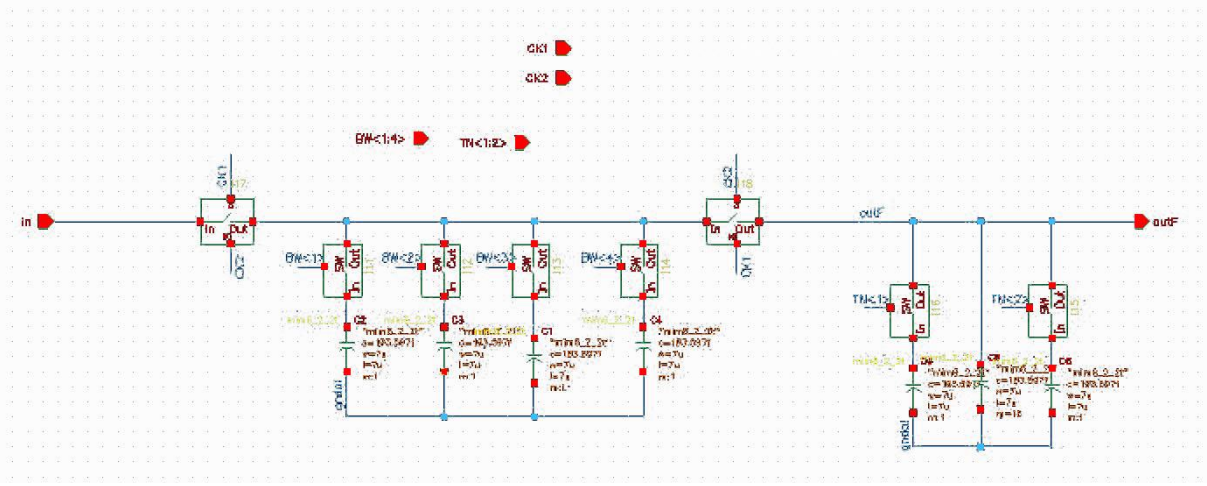

Figure 7.8 Tunable low-pass filter

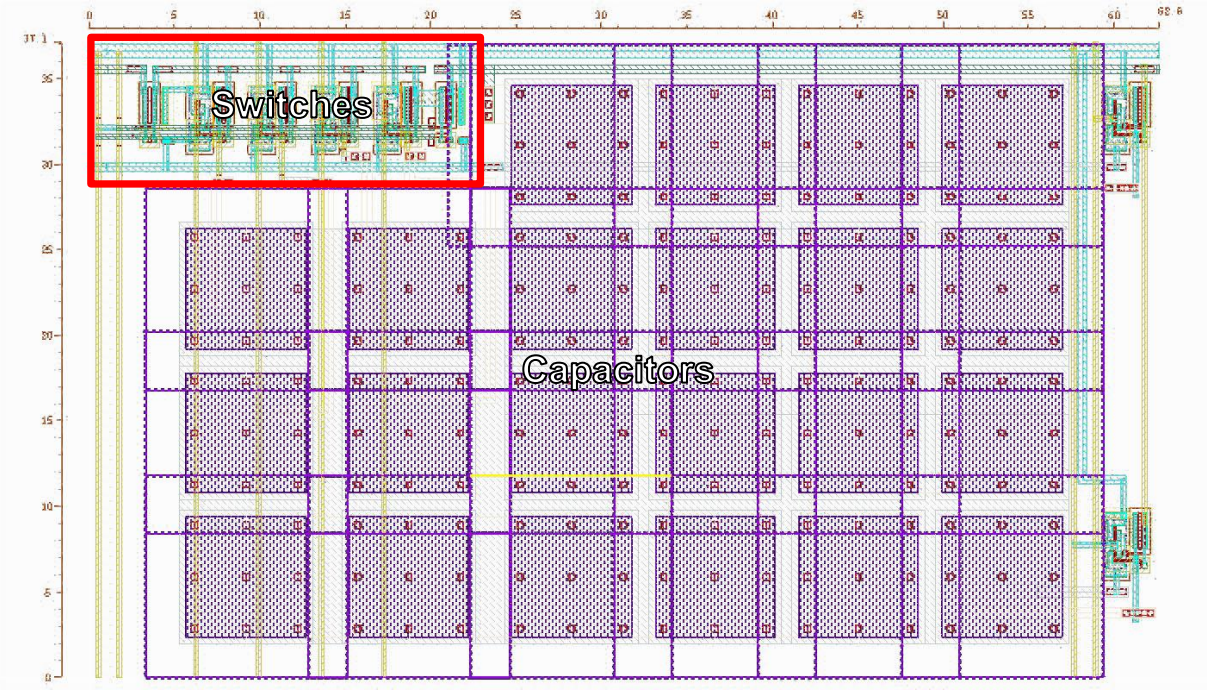

Figure 7.9 Layout low-pass filter

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The comparison between the active and passive 2nd order filter can be seen on Table 7.2.

	Band	Size [µm²]	Noise [µV]	Power [µW]
ACTIVE	AP	50 x 220	50	1.13
ACTIVE	LFP	50 x 220	27	1.13
PASSIVE	AP	40 x 250	28	0.0015
PASSIVE	LFP	40 x 120	19	0.0015

Table 7.3 2nd order active and passive filter comparison

The designed laboratory setup can be seen on figure 7.10. It shows structure of the probe, the head stage and the backend. The probe used to examine the thalamocortical activity. The typical placement on a rat is demonstrated on figure 7.11.

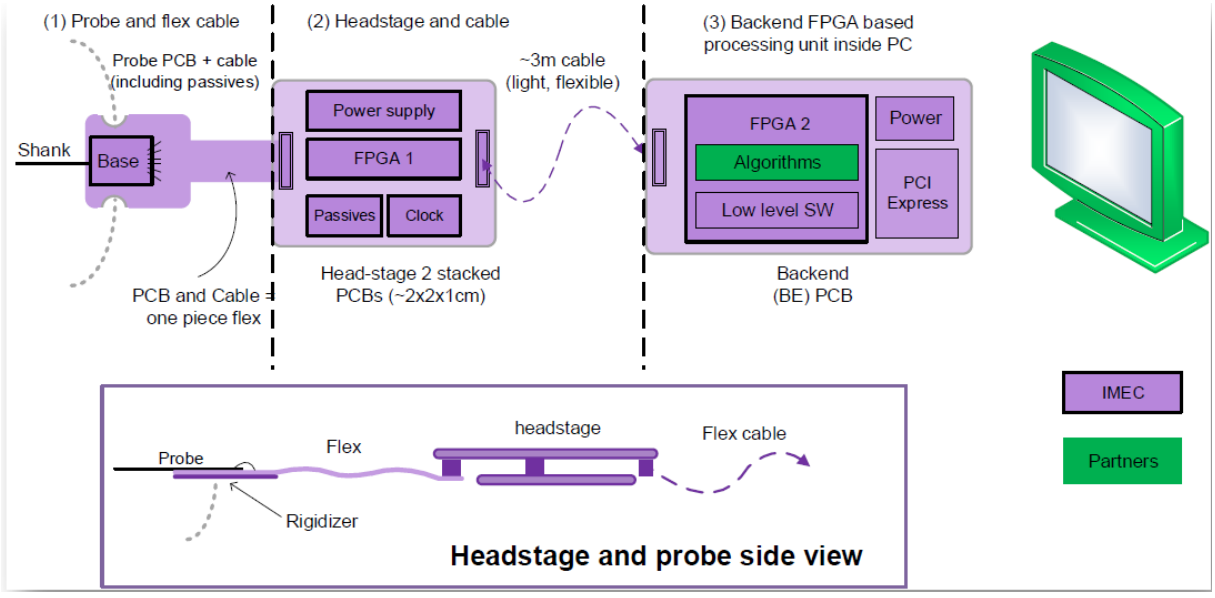

Figure 7.10 Advanced probe system concept

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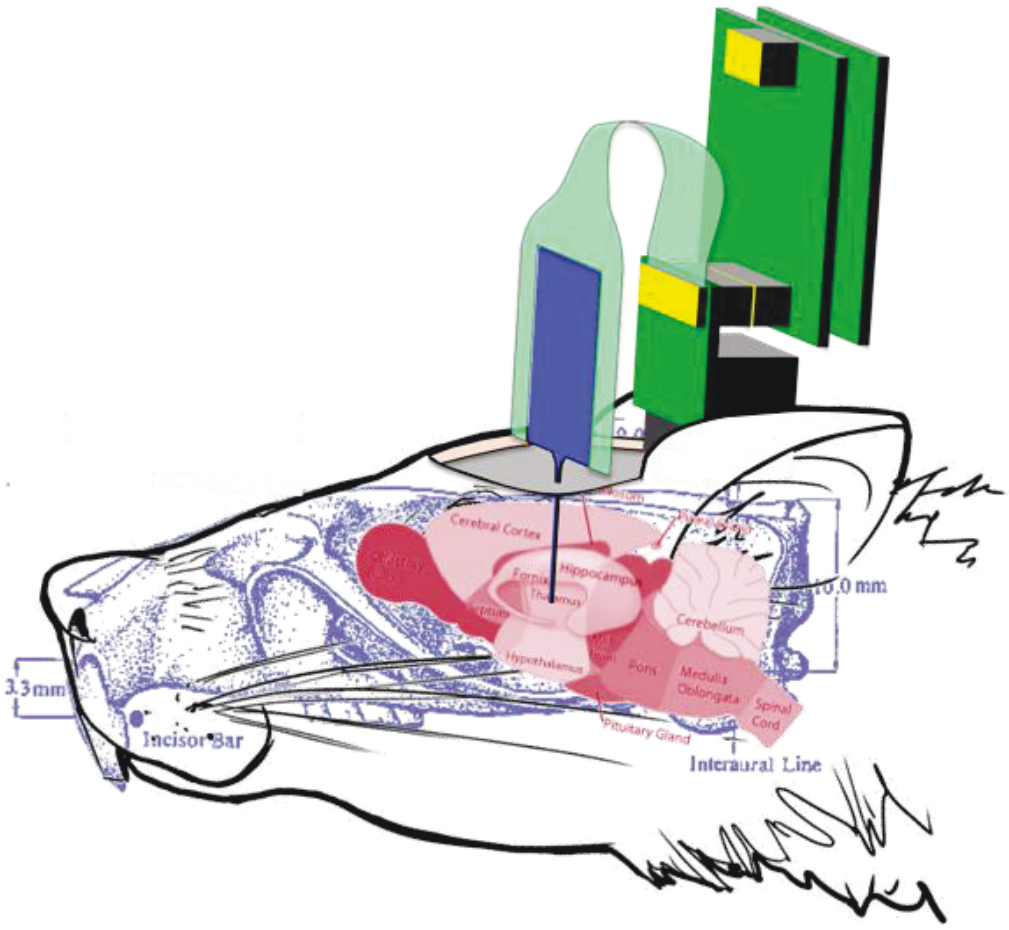

Figure 7.11 Rat recording setup

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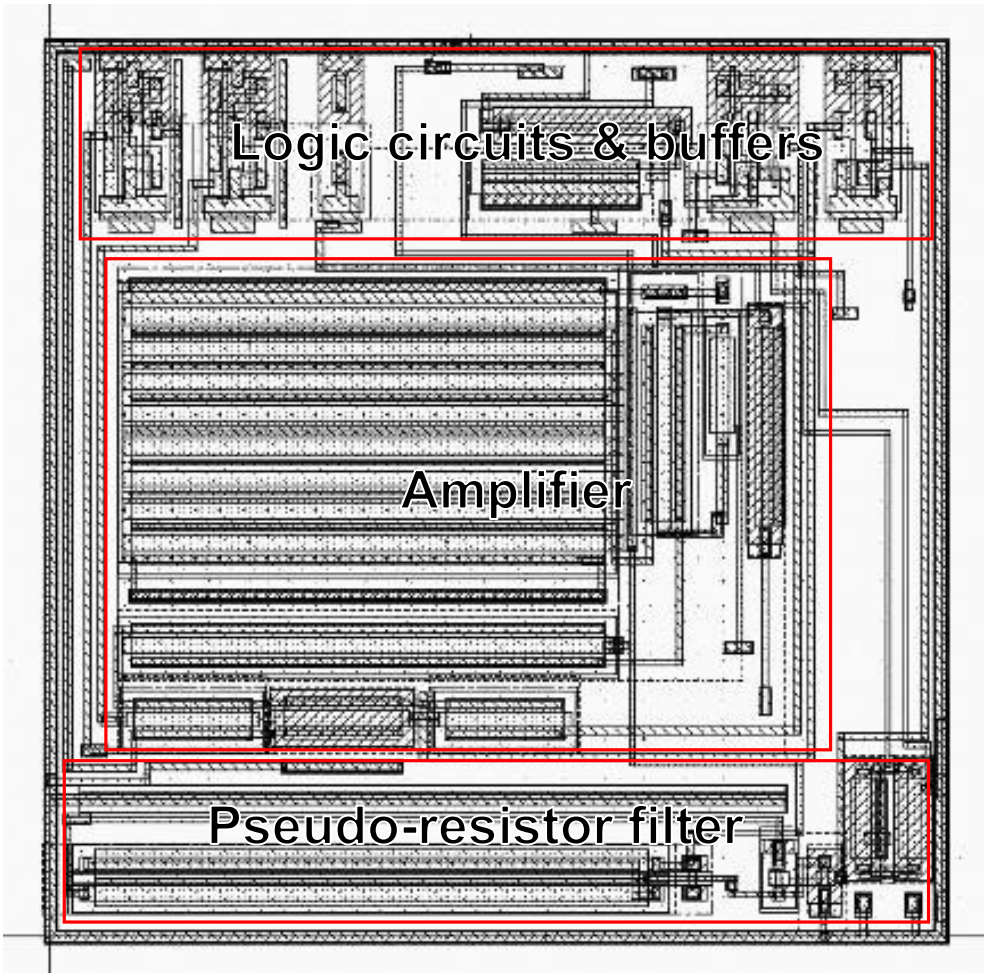

Figure 7.12 Layout of the advanced probe pixel architecture

Each pixel amplifier block contains an amplifier, a pseudo-resistor based passive filter and logic elements (Fig. 7.12).

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IX. ACKNOWLEDGEMENT

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X. THESIS 1

1.1

I proved that the generalized use of active pseudo resistors using extreme high-value resistors cannot be realized, which however is fundamentally important in the application of very low-frequency RC amplifiers' feedback loop. The broadband behavior of pseudo resistors causes low frequency distortion which prevents accurate measurement. The analysis of these low frequency distortions in neural amplifiers that use pseudo resistance hasn't been addressed before in the literature. [A1, A4]

1.2

I developed a design process for broadband extreme high-value and low distortion active resistors. The essence of the design process is the chaining of appropriately sized and suitably controlled pseudo MOS resistors, taking into account the scattered parasitic capacity, to minimize the distortion of the resistances and to optimize the noise in the system. [A1]

1.3

I developed two methods which are suitable for self-compensating the pseudo-resistance chains which were introduced in the previous (1.2) thesis point. The distortion caused by the active pseudo resistors can be further reduced using symmetry or current mirror based architectures. [A1]

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XI. THESIS 2

2.1

I developed a design procedure for high sensitivity neurobiological measurements, which with certain conditions such as allowed dissipation and size limits, achieves optimal input referred noise amplification with comparable noise and power consumption coefficient to other amplifiers for live animal measurements in laboratory. The architecture and the operation parameters were proved by measuring a chip manufactured by the Austrian Microsystems 0.35 µm stripe width Bi-CMOS technology. [A2, A3]

2.2

During the design process that was developed and described in thesis 2.1, I compared the low noise amplifier parameters using CMOS and Bi-CMOS technologies. The comparison proved that amplifiers fabricated on CMOS operate with less noise under similar size and power consumption. The tests chips were manufactured with the AMS 0.35 µm technology. [A2]

2.3

After examining the leading international journals with over two hundred articles published between 1997 and 2015 on the subject of neural signal low noise amplification, I concluded that, based on the published specifications for the technology I used, the amplifier implemented according to the established design method has better noise parameters. [A2]

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